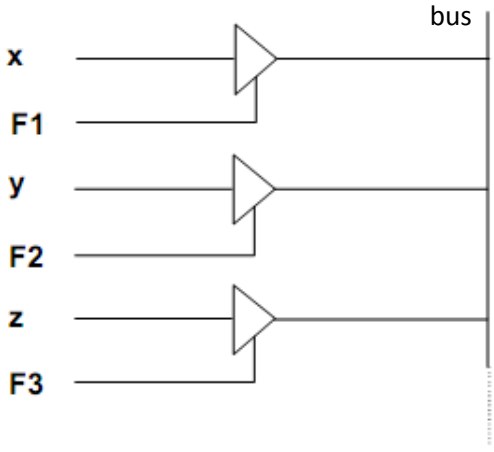
Digital Systems (Exam)
(TI2720-B)

Monday 5 November 2012 (09:00 – 12:00)

Directions for filling in the answer sheet:
- Fill in the answer sheet using a pencil (eraser allowed) or ballpoint. (ensure high enough contrast when "coloring" the boxes)
- Do not forget your name, student number, and signature.
- Fill in your student number in code also and double check.
- In case an answer is unknown it is better to guess than to leave open.
- Do not fill in the code figures in the lower right corner.
- **Start with answering the "easiest" questions first!!**
- In case you do not understand a question, ask the lecturer present.
- In case of cheating, no grade will be given and you will be reported.

Opgave 1: (Question 1)



Een drietal willekeurige signalen x, y en z zijn via TRI-state buffers met een buslijn verbonden, zoals hiernaast getekend. Er zijn 2 stuurfuncties gegeven, nl.:
F1 = A.B' en F2 = B.C.(A'+D')
Welke stuurfunctie F3 kan worden gebruikt zodat de schakeling correct kan werken?
(English: Three random signals x, y, and z are connected to a bus-line via TRI-state buffers (see figure). 2 driver functions are given as follows: F1 = A.B' and F2 = B.C.(A'+D') . Which driver function F3 can be used that ensures correct functioning of the given circuit?)

a. A.B.C b. B.C.D c. A.C'.D' d. A.B.D

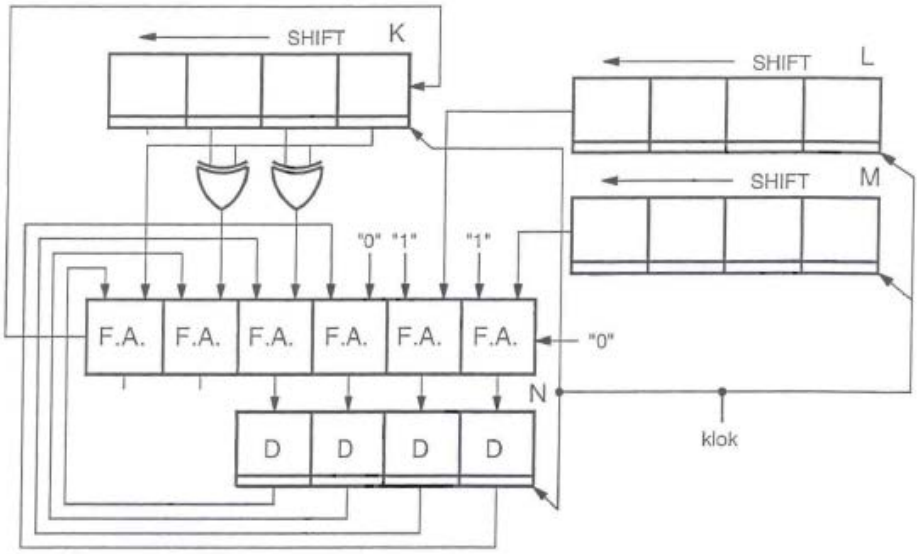
Opgave 2: (Question 2)

Beschouw de functie (x0 ⊕ x1) + (x2 ⊕ x3) en bepaal het aantal priemimplicanten (PI) en het essentiële aantal priemimplicanten (EPI).
(English: Consider the function (x0 ⊕ x1) + (x2 ⊕ x3) and determine the number of prime implicants (PI) and the number of essential prime implicants (EPI).)
a. 4 PI & 4 EPI b. 4 PI & 2 EPI c. 5 PI & 4 EPI d. 5 PI & 3 EPI

Opgave 3: (Question 3)

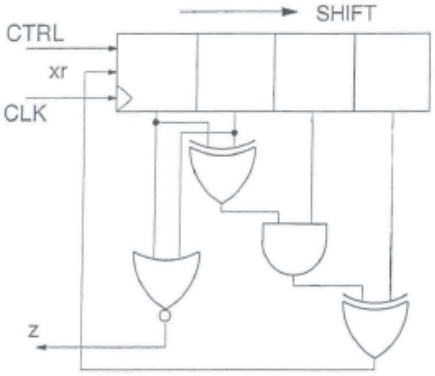
De expressie (x0 ⊕ x1).(x2 ⊕ x3) kan herschreven worden tot:
(English: The expression (x0 ⊕ x1).(x2 ⊕ x3) can be rewritten to:)
a. (x0 + x2) ⊕ (x1 + x2) ⊕ (x0 + x3) ⊕ (x1 + x3)
b. (x0'+x1') ⊕ (x2'+x3')
c. x0.x2 + x0.x3 + x1.x2 + x1.x3
d. x0'.x1 + x0.x1' + x2'.x3 + x2.x3'

Opgave 4: (Question 4)



Gegeven is een synchrone sequentiële schakeling (zie hierboven). De schakeling bestaat uit 3 schuifregisters K, L en M, een parallel load register N (4 secties), een full-adder (6 secties) en een tweetal poorten. Voor de startinhouden geldt: K = 0 0 0 0 , L = 1 0 0 1 , M = 0 0 1 1 en N = 1 1 1 1. Wat is na 4 klokpulsen de inhoud van register K?
(English: A sequential circuit (as depicted above) is given. The circuit comprises 3 shift registers K, L, and M, a parallel load register (4 sections), a full adder (6 sections), and two logical gates. The initial content of the registers are: K = 0 0 0 0 , L = 1 0 0 1 , M = 0 0 1 1 en N = 1 1 1 1. What is the content of register K after 4 clock cycles?)
a. 1 0 0 1 b. 0 1 1 0 c. 1 1 0 1 d. 1 0 1 1

Opgave 5: (Question 5)



Van nevenstaand schema zijn voor de poorten de volgende tijden gegeven: (English: For logical gates in the given circuit, the following timings are given:)

delay XOR : 11 nsec.
delay NOR : 15 nsec.
delay AND : 9 nsec.

En voor het schuifregister: (English: And for the shift register:)

setup time : 4 nsec.
hold time : 2 nsec.
propagation time : 10 nsec.

Wat is de maximale klokfrequentie waarbij het system nog goed kan werken? (English: What is the maximum clock frequency at which this system can still correctly operate?)
a. 29 MHz b. 24 MHz c. 22 MHz d. 21 MHz

Opgave 6: (Question 6)

PS	x=0	x=1
A	C,0	L,0
B	C,0	L,1
C	B,0	J,0
D	A,0	H,0
E	G,0	E,0
F	A,0	H,0
G	B,0	J,0
H	K,0	F,0
I	I,0	D,0
J	K,0	F,0
K	I,0	D,0
L	G,0	E,0

NS, z

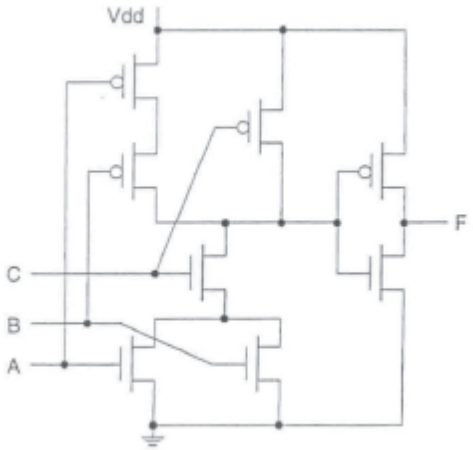
Gegeven het volgende toestandsdiagram: (English: Given the following state diagram:)

Hierin is x een input en z een output en x,z ∈ {0,1}. (English: Within, x is an input and z an output and x,z ∈ {0,1}.)

Welk paar toestanden is **wel** 3-equivalent, maar **niet** 4-equivalent?
(English: Which pair of states **is** 3-equivalent, but **not** 4-equivalent?)

a. F en/and L
b. F en/and J
c. E en/and L
d. E en/and J

Opgave 7: (Question 7)



Nevenstaand schema geeft de opbouw van een logische functie met MOS transistoren weer. Wat is de bij dit schema behorende formule?
(English: The given circuit depicts a logical function built using MOS transistors. What is corresponding logical expression?)

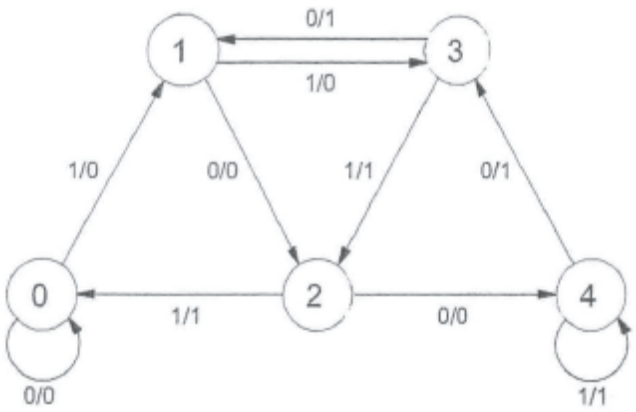
a. A.B + C
b. (A + B).C
c. A'.B' + C'
d. (A' + B').C'

Opgave 8: (Question 8)

Een teller T bestaande uit 3 T-flipflops T2, T1 en T0, waarvan T0 de laagstwaardige sectie is, doorloopt de getallen 0,5,2,7,4,1,6,3,0,… Dus S(i+1) = S(i) + 5 (mod 8). De uitgangssignalen van de flipflops zijn t2, t1 en t0, respectievelijk. Wat is dan de aansturing van T-flipflop T1?
(English: A counter T comprising 3 T-flipflops T2, T1, and T0, of which T0 is the least significant section, goes through the following values 0,5,2,7,4,1,6,3,0,… I.e., S(i+1) = S(i) + 5 (mod 8). The output signals of the flipflops are t2, t1, and t0, respectively. What is function to drive flipflop T1?)

a. t0 b. t0+t1 c. t0⊕t1 d. t1

Opgave 9: (Question 9)



In nevenstaand figuur is het diagram van een FSM gegeven. Wat is de outputstring u0,u1,u2,… als de inputstring i0,i1,i2,… (met i0 als eerste) = 11100100? De beginstand is toestand 0.
(English: An FSM is presented in the given diagram. What is the output string u0,u1,u2,… when the input string i0,i1,i2,… (with i0 as the first input) = 11100100? The starting state is state 0.
a. 00101101 b. 00101110
c. 00101111 d. 00101100

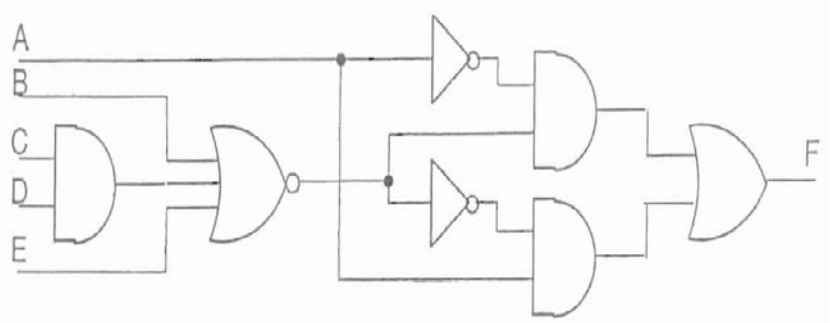
Opgave 10: (Question 10)

Gegeven de volgende VHDL code waarin een full adder wordt gemodelleerd. Hierin wordt gebruik gemaakt van twee half adders en een or-poort.
(English: Given is the VHDL code below in which a full is being modeled using two half adders and an or-gate.)

```
entity half_adder is
      generic (gate_delay : Time := 6 ns);
      port (a, b : in bit;  sum, carry : out bit);
end half_adder;

architecture my_half_adder_arch of half_adder is
begin
      carry <= a and b after 5 ns;
      sum   <= a exor b after gate_delay;
end my_half_adder_arch;

entity full_adder is
      generic (gate_delay : Time := 4 ns);
      port (a, b, c_in : in bit; sum, carry : out bit);
end full_adder;

architecture structural of full_adder is
      component half_adder is
            generic (gate_delay : Time := 6 ns);
            port (a, b : in bit; sum, carry : out bit);
      end component;
      signal s1, s2, s3 : bit;
begin
H1: half_adder      generic map (gate_delay => gate_delay)
                    port map (a => a, b => b, sum => s1, carry => s3);
H2: half_adder      port map (a => s1, b => c_in, sum => sum, carry => s2);
carry <= s2 or s3 after 5 ns;
end structural;
```

Wat is de langste delay (in ns) in de full adder van de ingangen naar de uitgangen in de gegeven code? (English: What is the longest delay (in ns) of the given full adder (written in VHDL) from the inputs to the outputs?)
a. 10 ns b. 13 ns c. 14 ns d. 16 ns

Opgave 11: (Question 11)



Wat is de netwerkvertraging $\mathbf{t_{pHL}}$ van nevenstaande schakeling als gegeven is dat de output load van de schakeling 1 is ? (Maak gebruik van de tabel op deze pagina)

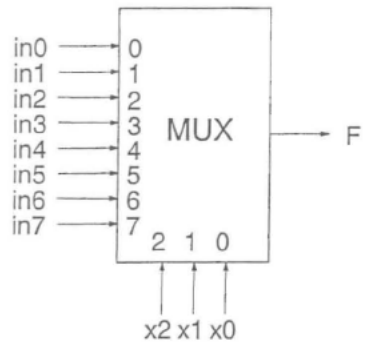
(English: What is the network propagation delay $\mathbf{t_{pHL}}$ of the given circuit when it is assumed that the output load of the circuit is 1? (Make use of the table below))

a. 0.737 ns
b. 0.854 ns
c. 0.911 ns
d. 1.022 ns

Characteristics of a family of CMOS gates

Gate Type	Fan in	Propagation Delays t_{pLH} (ns)	Propagation Delays t_{pHL} (ns)	Load Factor I (standard loads)	Size (equivalent gates)
AND	2	0.15 + 0.037L	0.16 + 0.017L	1.0	2
AND	3	0.20 + 0.038L	0.18 + 0.018L	1.0	2
AND	4	0.28 + 0.039L	0.21 + 0.019L	1.0	3
OR	2	0.12 + 0.037L	0.20 + 0.019L	1.0	2
OR	3	0.12 + 0.038L	0.34 + 0.022L	1.0	2
OR	4	0.13 + 0.038L	0.45 + 0.025L	1.0	3
NOT	1	0.02 + 0.038L	0.05 + 0.017L	1.0	1
NAND	2	0.05 + 0.038L	0.08 + 0.027L	1.0	1
NAND	3	0.07 + 0.038L	0.09 + 0.039L	1.0	2
NAND	4	0.10 + 0.037L	0.12 + 0.051L	1.0	2
NAND	5	0.21 + 0.038L	0.34 + 0.019L	1.0	4
NAND	6	0.24 + 0.037L	0.36 + 0.019L	1.0	5
NAND	8	0.24 + 0.038L	0.42 + 0.019L	1.0	6
NOR	2	0.06 + 0.075L	0.07 + 0.016L	1.0	1
NOR	3	0.16 + 0.111L	0.08 + 0.017L	1.0	2
NOR	4	0.23 + 0.149L	0.08 + 0.017L	1.0	4
NOR	5	0.38 + 0.038L	0.23 + 0.018L	1.0	4
NOR	6	0.46 + 0.037L	0.24 + 0.018L	1.0	5
NOR	8	0.54 + 0.038L	0.23 + 0.018L	1.0	6
XOR	2*	0.30 + 0.036L	0.30 + 0.021L	1.1	3
		0.16 + 0.036L	0.15 + 0.020L	2.0	
XOR	3*	0.50 + 0.038L	0.49 + 0.027L	1.1	6
		0.28 + 0.039L	0.27 + 0.027L	2.4	
		0.19 + 0.036L	0.17 + 0.025L	2.1	
XNOR	2*	0.30 + 0.036L	0.30 + 0.021L	1.1	3
		0.16 + 0.036L	0.15 + 0.020L	2.0	
XNOR	3*	0.50 + 0.038L	0.49 + 0.027L	1.1	6
		0.28 + 0.039L	0.27 + 0.027L	2.3	
		0.19 + 0.036L	0.17 + 0.025L	1.3	
2-OR/NAND2	4	0.17 + 0.075L	0.10 + 0.028L	1.0	2
2-AND/NOR2	4	0.17 + 0.075L	0.10 + 0.028L	1.0	2

Opgave 12: (Question 12)



Met behulp van een multiplexer wordt een F(x3,x2,x1,x0) = (x0⊕x1.x2')⊕(x0.x2'+x1.x3) gemaakt. Wat moet er aan de ingangen respectievelijk worden aangesloten?
in0,in1,in2,in3,in4,in5,in6,in7 =
(English: Using a multiplexer the function F(x3,x2,x1,x0) = (x0⊕x1.x2')⊕(x0.x2'+x1.x3) is being realized. What has to be provided at the inputs, respectively?
in0,in1,in2,in3,in4,in5,in6,in7 =

a. 0,0,x3',x3,1,0,1,x3' b. 0,x3',0,x3,0,1,1,x3'
c. 0,0,0,1,x3',x3,1,x3' d. 0,0,x3',1,0,1,x3,x3'

Opgave 13: (Question 13)

Van de decimale getallen 82 en -35 worden de two's complement gecodeerde vormen in een 8 secties tellende full-adder bij elkaar opgeteld. Hoeveel **interne** carry's in de full-adder krijgen de waarde 1?
(English: Two decimal numbers 82 and -35, represented in 2's complement notation, are being added by an full-adder with 8 sections. How many **internal** carry's within the full-adder become 1?)
a. 1 b. 2 c. 3 d. 4

Opgave 14: (Question 14)

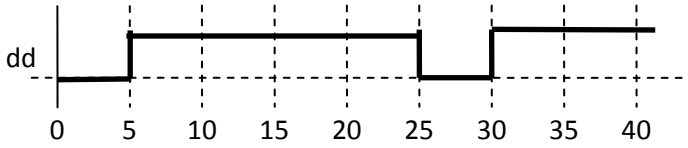
Bij het coderen van getallen wordt de BCD-code gebruikt. Elk woord van 16 bits bestaat uit 4 BCD cijfers. Hoeveel code combinaties worden er, per woord, op die manier **niet** gebruikt?
(English: In the coding of numbers the BCD-code is being utilized. Each word of 16 bits comprises 4 BCD values. How many code combinations (per word) are not being utilized in this way?)
a. 1296 b. 24576 c. 26214 d. 55536

Opgave 15: (Question 15)

```
entity boolean_test is
end boolean_test;

architecture gedrag of boolean_test is
      component boolean_functie is
            port (a, b, c : in bit; uit : out bit);
      end component;
      signal aa, bb, cc, dd ; bit;
begin
      N1: boolean_functie port map (aa, bb, cc, dd);
      aa <= '1', '0' after 5 ns, '1' after 15 ns, '1' after 30 ns, '1' after 35 ns, '0'
            after 40 ns;
      bb <= '0', '1' after 10 ns, '0' after 20 ns, '1' after 35 ns;
      cc <= ...   – deze regel moet nog worden ingevuld
end gedrag;
```

De component boolean_functie is niet gegeven in VHDL, maar wel gegeven als een product van maxtermen F(a,b,c) = Π M(1,2,5,7). Verder is het de bedoeling dat de component de volgende uitgang realiseert: (English: The component boolean_functie is not given in VHDL, but as a product of

maxterms F(a,b,c) = Π M(1,2,5,7). Furthermore, the component should produce the following waveform as output:)



Welke van de vier onderstaande statements moet worden ingevuld als waveform van signaal cc om de gevraagde signaal dd te genereren? (English: Which of the four following statements should be used for signal cc in order to generate signal dd?)

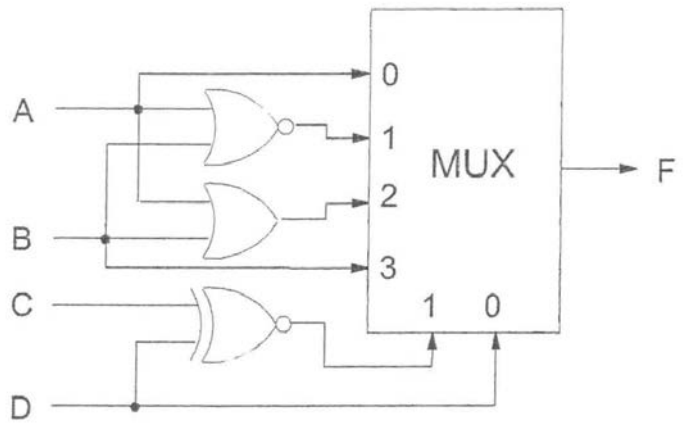
a. cc <= '0', '1' after 15 ns, '0' after 20 ns, '1' after 25 ns, '0' after 30 ns, '1' after 35 ns;
b. cc <= '1', '0' after 10 ns, '1' after 15 ns, '0' after 25 ns, '1' after 30 ns, '0' after 40 ns;
c. cc <= '1', '0' after 5 ns, '1' after 10 ns, '0' after 15 ns, '1' after 25 ns, '0' after 30 ns, '1' after 40 ns;
d. geen van de bovenstaande antwoorden. (English: none of the above.)

Opgave 16: (Question 16)

In een schakeling met 3 D-flipflops A, B en C wordt de D-ingang van flipflop B bestuurd door een signaal met formule A.B+C' . Als deze D-flipflop door een JK-flipflop wordt vergangen, wat zijn dan de formules voor de J- en voor de K-ingang van flipflop B?
(English: In a circuit with 3 D-flipflops A, B, and C, the D-input of flipflop B is driven by a signal with the expression A.B+C' . If this D-flipflop is replaced by a JK-flipflop, what are the expressions for the J- and K-input of flipflop B?)

	J	K
a.	A.B + C'	C' + A.B
b.	A + C'	C
c.	A.B	C.(A' + B')
d.	C'	A'.C

Opgave 17: (Question 17)



Bepaal de **maxterm**vorm van F(D,C,B,A):
(English: Determine F(D,C,B,A) in terms of **maxterms**:)

a. Π M(0,4,6,9,10,11,12,13)
b. Π M(0,2,4,8,9,13,14,15)
c. Π M(0,4,6,8,10,12)
d. Π M(0,2,4,9,10,11,12,13)

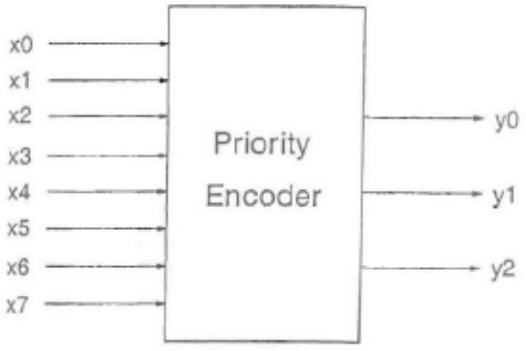
Opgave 18: (Question 18)

Om een "6-naar-64 decoder" samen te stellen zijn 2 typen chips beschikbaar, nl. type A: met daarin 2 "2-naar-4 decoder"s, en type b: met daarin 1 "3-naar-8 decoder". Hoeveel chips zijn er respectievelijk van type A of van type B nodig? (Er mag niet worden gemixed) (English: In order to build a "6-to-64 decoder", we can make use of two types of chips, namely type A: containing 2 "2-to-4 decoder"s, and type B: containing 1 "3-to-8 decoder". How many chips are needed when only type A or type B, respectively, are allowed to be used? (Both types cannot be mixed))

	Type A	Type B
a.	8	8
b.	9	9
c.	11	9
d.	11	8

Opgave 19: (Question 19)

De ingangen van nevenstaande priority encoder worden als volgt aangesloten: (English: The inputs of the given circuit are connected as follows:)

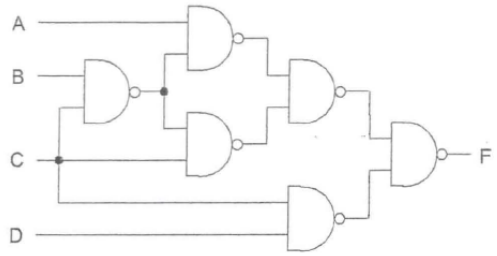


x0 = 1
x1 = t2′
x2 = t1′
x3 = t1′.t2′
x4 = t0′
x5 = t0′.t1′
x6 = t0′.t2′
x7 = t0′.t1′.t2′

Hierin komen de signalen ti van een binaire teller met t0 als laagstwaardigste en t2 als hoogstwaardigste bit. Als de binaire teller de standen 0 t/m 7 doorloopt, welke reeks getallen zien we dan bij de output Y (= y2 y1 y0)?
(English: Herewithin the signals ti are coming from a binary counter with t0 as the least significant and t2 as the most significant bit. If the binary counter counts from 0 till 7 (inclusive), which series of numbers will be presented at the output Y (= y2 y1 y0)?)

a. 7 5 4 3 2 1 0 0
b. 7 4 1 6 3 0 5 2
c. 7 3 6 1 5 2 4 0
d. 7 6 5 4 2 3 1 0

Opgave 20: (Question 20)



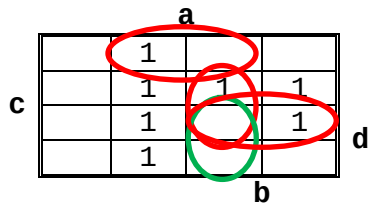
In nevenstaand schema is een schakeling met poorten gegeven. Welke van onderstaande formules geeft F weer? (English: In the given circuit a network of gates is presented. Which of the following expressions represents function F?)

a. A′.B + C.D + B.C
b. A′.C′+ B.C + C.D
c. A′.B + C.D + A′C′
d. A′.C′+ B.C + A′.B

Antwoorden en Uitwerkingen (Answers)

Opgave		Opgave		Opgave		Opgave	
1	D	6	B	11	D	16	D
2	A	7	B	12	D	17	A
3	A	8	A	13	B	18	C
4	D	9	A	14	D	19	C
5	C	10	C	15	C	20	B

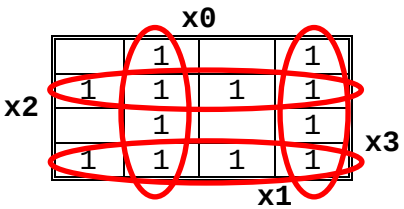
Question 1: (d)



The only expression (in green) that does not overlap with any of the earlier functions F1 or F2 is A.B.D → answer d.

Question 2: (a)

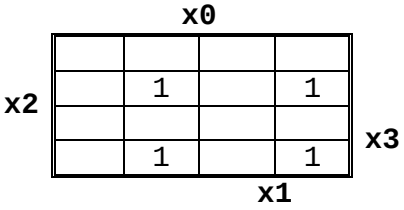
The given function leads to the following K-map:



From this K-map, we can identify four PIs and all of them are essential as they contain ones that are not covered by other PIs.

Question 3: (a)

The given expression can be rewritten as follows:
(x0’.x1 + x0.x1’).(x2’.x3 + x2.x3’) =
x0’.x1.x2’.x3 + x0’.x1.x2.x3’ + x0.x1’.x2’.x3 + x0.x1’.x2.x3’
resulting in the following K-map:



Answers c. and d. are clearly wrong by simply imagining those expressions in the given K-map. When considering answer b., we can quickly draw 2 K-map for the expressions (x0’+x1’) and (x2’+x3’) and performing the exor operation on the K-maps (i.e., count the odd number of ones per cell). This will result in an incorrect answer too. Answer a. can be verified in the same way by drawing 4 K-maps and counting the odd number of ones per cell.

Question 4: (d)
In this question, you have to do some bookkeeping of the register per cycle and determine the inputs and outputs of the full adders that in turn determine the new content of the registers. If you have done this correctly, you should arrive at answer d.

Question 5: (c)
We have to derive the longest path of the combinational circuit and include the setup time and propagation time of the register. This will result in: 11+9+11+4+10 = 45 nsec. Calculating the inverse, we can obtain the frequency, i.e.: 22.2 MHz. This means we cannot clock the system higher than this frequency and the closest match is 22 MHz → answer c.

Question 6: (b)
1-equivalence:
(A, C, D, E, F, G, H, I, J, K, L) (B)
2-equivalence:
(A, D, E, F, H, I, J, K, L) (C, G) (B)
3-equivalence:
(D, F, H, I, J, K) (A, E, L) (C, G) (B)
4-equivalence:
(H, I, J, K) (D, F) (A, E, L) (C, G) (B)

The answer can now be easily derived.

Question 7: (b)

Question 8: (a)
Based on the information given in the question, we can derive the following truth table that determines the new inputs of the flipflops. We first assume a D-flipflop D1 for T1 and then derive whether the state should be flipped – this will give us the function to drive the T1 input.

Previous State (PS)			Next State (NS)			
T2 (t2)	T1 (t1)	T0 (t0)	D2	D1	D0	T1
0	0	0	1	0	1	0
0	0	1	1	1	0	1
0	1	0	1	1	1	0
0	1	1	0	0	0	1
1	0	0	0	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	1	0	0	1

From this table, we can see that T1 = t0.

Question 9: (a)

Question 10: (c)
The longest path runs from the “exor” of H1 (=4 ns), the “and” of H2 (=5 ns), and the last “or” (=5 ns). This results in 14 ns.

Question 11: (d)

Tp(HL)(OR2) + Tp(HL)(AND2) + Tp(HL)(NOT) + Tp(LH)(NOR3) + Tp(HL)(AND2) = 0.219 + 0.177 + 0.67 + 0.382 + 0.177 = 1.022

Question 12: (d)

					A	B	C	D	
j	x2	x1	x0	x1.x2′	x0⊕x1.x2′	x0.x2′	x1.x3	B+C	A⊕D
0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	1	0	1	0
2	0	1	0	1	1	0	x3	x3	x3′
3	0	1	1	1	0	1	x3	1	1
4	1	0	0	0	0	0	0	0	0
5	1	0	1	0	1	0	0	0	1
6	1	1	0	0	0	0	x3	x3	x3
7	1	1	1	0	1	0	x3	x3	x3′

Question 13: (b)

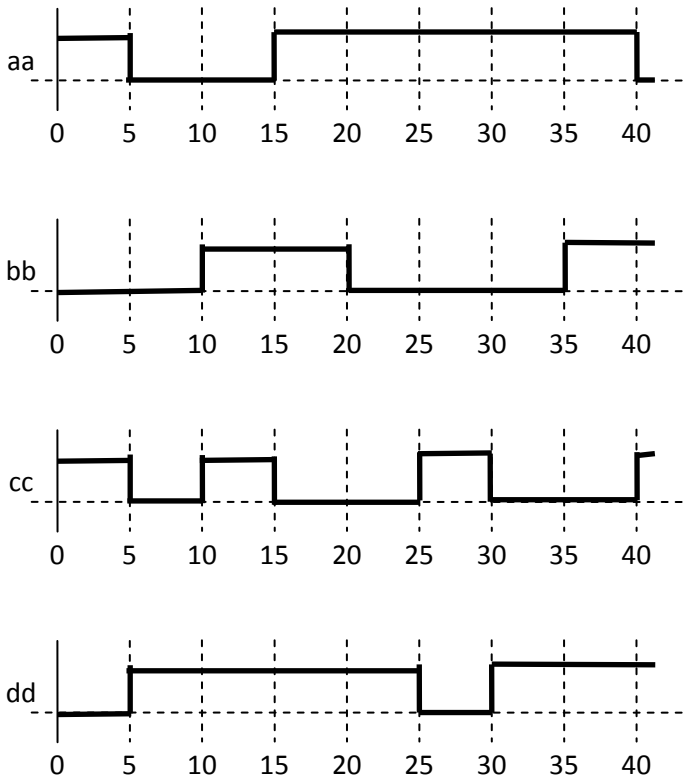
82 = 0 1 0 1 0 0 1 0
-35= 1 1 0 1 1 1 0 1 +
47 = 0 0 1 0 1 1 1 1

I.e., 2 internal carrys.

Question 14: (d)

2^{16} – 10000 = 65536 – 10000 = 55536

Question 15: (c)



The truth table of function F is:

j	a	b	c	d
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	0

Question 16: (d)

Assuming a D-flipflop, the given expression can be put in K-map as:

c \ a,b	00	01	11	10
1	1	1	1	1
0	0	0	1	0

Using the excitation functions, we can generate K-maps for the J- and K-inputs.

J-input: = C′

c \ a,b	00	01	11	10
1	1	1	-	-
0	0	0	-	-

K-input: =A′C

c \ a,b	00	01	11	10
-	-	-	0	0
-	-	-	0	1

Question 17: (a)

					Selectors		Mux Inputs				
					C xnor D	*D*	*A*	*A nor B*	*A or B*	*B*	
J	**D**	**C**	**B**	**A**	**1**	**0**	**0**	**1**	**2**	**3**	**F**
0	0	0	0	0	1	0			0		
1	0	0	0	1	1	0			1		
2	0	0	1	0	1	0			1		
3	0	0	1	1	1	0			1		
4	0	1	0	0	0	0	0				
5	0	1	0	1	0	0	1				
6	0	1	1	0	0	0	0				
7	0	1	1	1	0	0	1				
8	1	0	0	0	0	1		1			
9	1	0	0	1	0	1		0			
10	1	0	1	0	0	1		0			
11	1	0	1	1	0	1		0			
12	1	1	0	0	1	1				0	
13	1	1	0	1	1	1				0	
14	1	1	1	0	1	1				1	
15	1	1	1	1	1	1				1	

Σ m(1,2,3,5,7,8,14,15) = Π M(0,4,6,9,10,11,12,13)

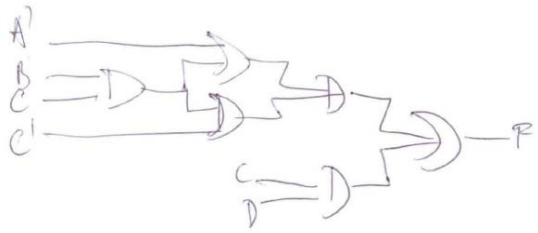
Question 18: (c)

Question 19: (c)

count	t2	t1	t0	x0	x1	x2	x3	x4	x5	x6	x7	Y
0	0	0	0	1	1	1	1	1	1	1	1	7
1	0	0	1	1	1	1	1	0	0	0	0	3
2	0	1	0	1	1	0	0	1	0	1	0	6
3	0	1	1	1	1	0	0	0	0	0	0	1
4	1	0	0	1	0	1	0	1	1	0	0	5
5	1	0	1	1	0	1	0	0	0	0	0	2
6	1	1	0	1	0	0	0	1	0	0	0	4
7	1	1	1	1	0	0	0	0	0	0	0	0

Question 20: (b)

The Morgan's law can be graphically applied to the last and second from last column resulting in:



This will result in B.C + A'.C' + C.D