Digital Systems (Exam)
(TI2720-B)

Monday 07 November 2011 (09:00 – 12:00)

Directions for filling in the answer sheet:
- Fill in answer sheet using a pencil (eraser allowed) or ballpoint.
  (ensure high enough contrast when "coloring" boxes)
- Do not forget your name, student number, and signature.
- Fill in your student number in code also and double check.
- In case an answer is unknown it is better to guess than leave open.
- Do not fill in the code figures in the lower right corner.
- **Start with answering the "easiest" questions first!!**
- In case you do not understand a question, ask the teacher present.
- In case of cheating, no grade will be given and you will be reported.

Opgave 1: (Question 1)

Gegeven de functie: (English: Given the function:)

F(A,B,C,D) = (A'+ B). (C'+ D). (A + B'+ C + D')

Hoeveel **priem-implikaten (PI)** en hoeveel **essentiële priem-implikaten (EPI)** zijn er in deze functie te vinden ? (English: How many **prime implicates (PI)** and how may **essential prime implicates (EPI)** can be identified in this function?)

a. 3 PI's en 3 EPI's
b. 4 PI's en 3 EPI's
c. 6 PI's en 0 EPI's
d. 8 PI's en 0 EPI's

Opgave 2: (Question 2)

Welk van de 4 volgende optellingen van 8 bits two's complement getallen zal een overflow geven? (English: Which of the following four additions of 8-bit 2's complement numbers will result in an overflow?)

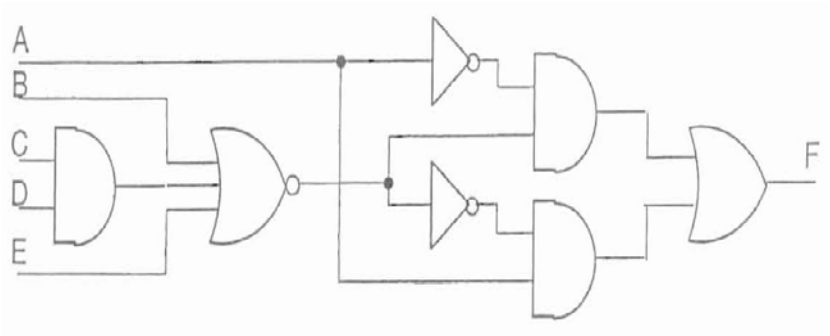
a.		b.		c.		d.	
10010000		00100000		10100000		00001111	
11110000	+	11110000	+	01111111	+	01110111	+

Opgave 3: (Question 3)

In VHDL worden naast signalen ook variabelen gebruikt. Welke van de volgende 4 beweringen is juist? (English: In VHDL, variables are being used next to signals. Which of the following 4 statements are correct?)

a. In een process body mogen alleen signalen worden gebruikt.
   (English: In a process body, only signals can be used.)
b. Variabelen komen alleen voor in functies en procedures.
   (English: Variables only occur in functions and procedures.)
c. Toekenning van een nieuwe waarde aan een variabele gebeurt pas een delta delay later.
   (English: Variables are assigned a new value after a delta delay.)
d. Geen van de bovenstaande beweringen is juist.
   (English: None of the above statements is correct.)

Opgave 4: (Question 4)



Wat is de netwerkvertraging t_{pLH} van nevenstaande schakeling als gegeven is dat de output load van de schakeling 1 is ? (Maak gebruik van de tabel op deze pagina)

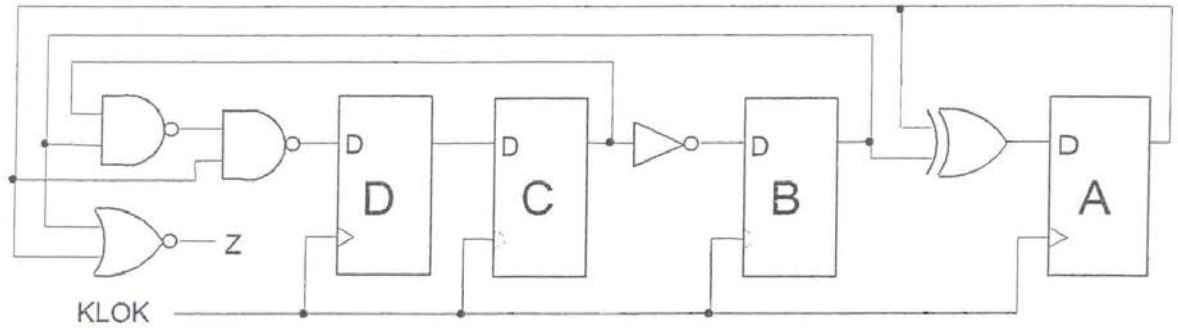
(English: What is the network propagation delay t_{pLH} of the given circuit when it is assumed that the output load of the circuit is 1? (Make use of the table below))

a. 0.686 ns
b. 0.703 ns
c. 0.860 ns
d. 0.971 ns

Characteristics of a family of CMOS gates

Gate Type	Fan in	Propagation Delays t_{pLH} (ns)	Propagation Delays t_{pHL} (ns)	Load Factor I (standard loads)	Size (equivalent gates)
AND	2	0.15 + 0.037L	0.16 + 0.017L	1.0	2
AND	3	0.20 + 0.038L	0.18 + 0.018L	1.0	2
AND	4	0.28 + 0.039L	0.21 + 0.019L	1.0	3
OR	2	0.12 + 0.037L	0.20 + 0.019L	1.0	2
OR	3	0.12 + 0.038L	0.34 + 0.022L	1.0	2
OR	4	0.13 + 0.038L	0.45 + 0.025L	1.0	3
NOT	1	0.02 + 0.038L	0.05 + 0.017L	1.0	1
NAND	2	0.05 + 0.038L	0.08 + 0.027L	1.0	1
NAND	3	0.07 + 0.038L	0.09 + 0.039L	1.0	2
NAND	4	0.10 + 0.037L	0.12 + 0.051L	1.0	2
NAND	5	0.21 + 0.038L	0.34 + 0.019L	1.0	4
NAND	6	0.24 + 0.037L	0.36 + 0.019L	1.0	5
NAND	8	0.24 + 0.038L	0.42 + 0.019L	1.0	6
NOR	2	0.06 + 0.075L	0.07 + 0.016L	1.0	1
NOR	3	0.16 + 0.111L	0.08 + 0.017L	1.0	2
NOR	4	0.23 + 0.149L	0.08 + 0.017L	1.0	4
NOR	5	0.38 + 0.038L	0.23 + 0.018L	1.0	4
NOR	6	0.46 + 0.037L	0.24 + 0.018L	1.0	5
NOR	8	0.54 + 0.038L	0.23 + 0.018L	1.0	6
XOR	2*	0.30 + 0.036L	0.30 + 0.021L	1.1	3
		0.16 + 0.036L	0.15 + 0.020L	2.0	
XOR	3*	0.50 + 0.038L	0.49 + 0.027L	1.1	6
		0.28 + 0.039L	0.27 + 0.027L	2.4	
		0.19 + 0.036L	0.17 + 0.025L	2.1	
XNOR	2*	0.30 + 0.036L	0.30 + 0.021L	1.1	3
		0.16 + 0.036L	0.15 + 0.020L	2.0	
XNOR	3*	0.50 + 0.038L	0.49 + 0.027L	1.1	6
		0.28 + 0.039L	0.27 + 0.027L	2.3	
		0.19 + 0.036L	0.17 + 0.025L	1.3	
2-OR/NAND2	4	0.17 + 0.075L	0.10 + 0.028L	1.0	2
2-AND/NOR2	4	0.17 + 0.075L	0.10 + 0.028L	1.0	2

Opgave 5: (Question 5)



Bovenstaand schema is opgebouwd uit 4 D-flipflops en enkele poorten, en heeft een uitgang z. Als de periodeduur van de klokpuls Tp is, wat is dan de tijdsduur tussen 2 opgaande flanken van het uitgangssignaal z uitgedrukt in Tp? (Hint: Start in stand DCBA = 0001)
(English: The circuit above comprises 4 D-flipflops and several gates, and an output z. Assuming that the clock period is Tp, what is the duration between two rising edges of the output signal z expressed in Tp? (Hint: Start in state DCBA = 0001))

a. 9 Tp b. 10 Tp c. 11 Tp d. 12 Tp

Opgave 6: (Question 6)

Van de schema gegeven in vraag 5 zijn voor de componenten de volgende tijden gegeven: (English: The timing and delays of the components used in Question 5 are given below:)

	D-flipflops
delay XOR: 10 nsec.	
delay NOR: 5 nsec.	setup tijd: 4 nsec.
delay NAND: 4 nsec.	holdtijd: 2 nsec.
delay INVERTER: 2 nsec.	omslagtijd: 5 nsec.

Welke van de onderstaande waarde kan als max. klokpulsfrequentie worden gekozen waarbij het systeem nog goed kan werken? (English: Which of the following frequencies can be used as the maximum frequency while ensuring that the circuit still functions correctly?)

a. 40 MHz b. 45 MHz c. 50 MHz d. 55 MHz

Opgave 7: (Question 7)

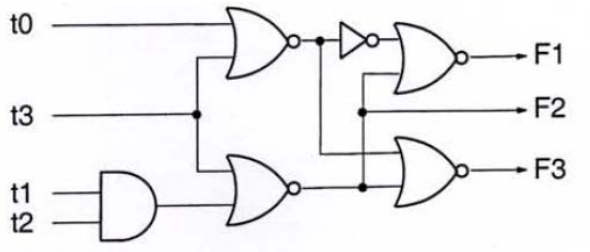
Met 64 geheugenchips van 1Mx4 en een aantal 2-input decoderchips wordt een zo groot mogelijk geheugensysteem voor woorden van 16 bits samengesteld. Hoeveel decoderchips zijn er voor dit systeem nodig?
(English: With 64 memory elements of size 1Mx4 and several 2-input decoder chips an as large as possible memory system with words of 16 bits is being built. How many decoder chips are needed for this system?)

a. 3 b. 4 c. 5 d. 8

Opgave 8: (Question 8)

Op een kruispunt wordt de besturing van de cyclus van twee stoplichten door een binaire teller geregeld. In onderstaande tabel is aangegeven welke lampen, R(rood), G(groen) of O(oranje) van de verkeerslichten L0 en L1 respectievelijk branden bij de opeenvolgende tellerstanden. Het onderstaande schema bestuurt de drie lampen van een der stoplichten. (English: At a traffic crossing, the color cycling of two traffic lights are being controlled by a binary counter. In the table below, the lights (R)ed, (G)reen, and (O)range of traffic lights L0 and L1 are lit respectively depending on the sequence of counter states. The circuit below controls the three lights of the traffic lights.)

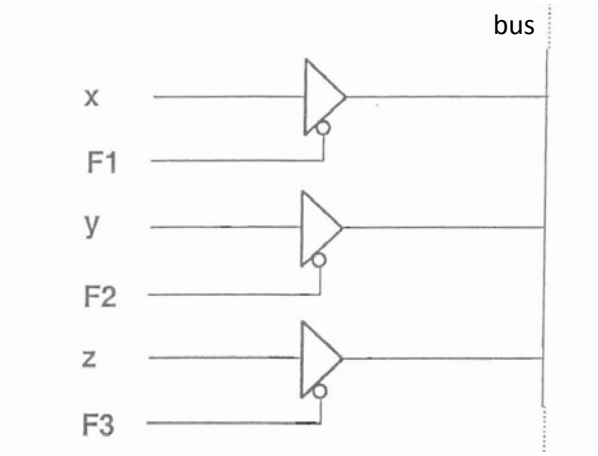
$t_{3-2-1-0}$	L0	L1	$t_{3-2-1-0}$	L0	L1
0000	G	R	1000	R	G
0001	G	R	1001	R	G
0010	G	R	1010	R	G
0011	G	R	1011	R	G
0100	G	R	1100	R	G
0101	G	R	1101	R	G
0110	O	R	1110	R	O
0111	R	R	1111	R	R



Welke uitgang Fx van de schakeling bestuurt de R(ode) lamp van L0? (English: Which output Fx controls the (R)ed light of traffic light L0?)

a. F1 b. F2 c. F3 d. geen (none)

Opgave 9: (Question 9)



Een drietal willekeurige signalen x, y en z zijn via TRI-state buffers met een bus verbonden, zoals hiernaast getekend. Er zijn 2 stuurfunkties gegeven nl.: Fl = B'+ D en F2 = A' .C'+ D' --- Welke stuurfunktie F3 kan gebruikt worden zodat de schakeling correct kan werken. (English: Three random signals x, y, and z are connected to a bus using TRI-state buffers (see figure). Two driver functions are given: Fl = B'+ D en F2 = A' .C'+ D' --- Which driver function F3 can be used to ensure correct functioning?)

a. A + B′ + C b. A + B + D′ c. A′ + C′ + D d. A′ + B + D

Opgave 10: (Question 10)

Een teller bestaande uit 4 D-flipflops D, C, B en A doorloopt cyclisch de toestanden DCBA volgens: 0001, 1010, 0101, 0111, 0011, 1110, 1001, 0010, 1100, 1101, 1111, 1011, 0110, 0001 enz. Hoe ziet in formule de aansturing van flipflop A eruit?

(English: A counter consisting of 4 D-flipflops D, C, B, and A cycles through the states DCBA according: 0001, 1010, 0101, 0111, 0011, 1110, 1001, 0010, 1100, 1101, 1111, 1011, 0110, 0001 etc. What is the expression to control flipflop A?)

a. $(C \oplus D)'$ b. $B' + C'$ c. A d. $C + A'.D$

Opgave 11: (Question 11)

Als toestandstabel is gegeven: (English: Given the following state table:)

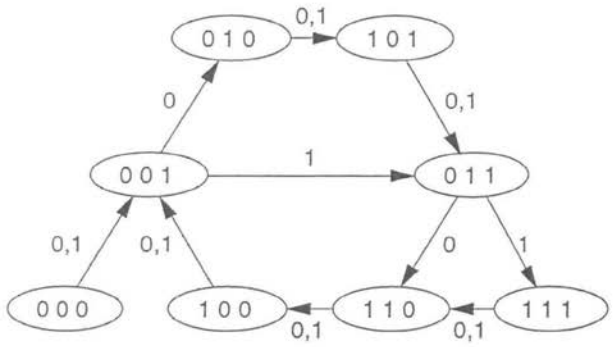
PS	x=0	x=1	x=2
A	I,0	C,0	D,0
B	H,0	F,0	E,0
C	A,0	I,0	D,0
D	J,1	B,1	F,1
E	J,0	B,0	G,0
F	H,0	G,0	B,0
G	J,0	E,0	F,0
H	J,0	B,0	D,0
I	C,0	A,0	D,0
J	H,0	F,0	D,0
	NS, z		

Hierin is x een input en z een output met $x,z \in \{0,1,2\}$. Welk tweetal toestanden is wel 2-equivalent, maar niet 3-equivalent?

(English: Here, x is the input and z is the output with $x,z \in \{0,1,2\}$. Which pair of states is 2-equivalent, but not 3-equivalent?)

a. H en I
b. H en J
c. C en A
d. C en I

Opgave 12: (Question 12)

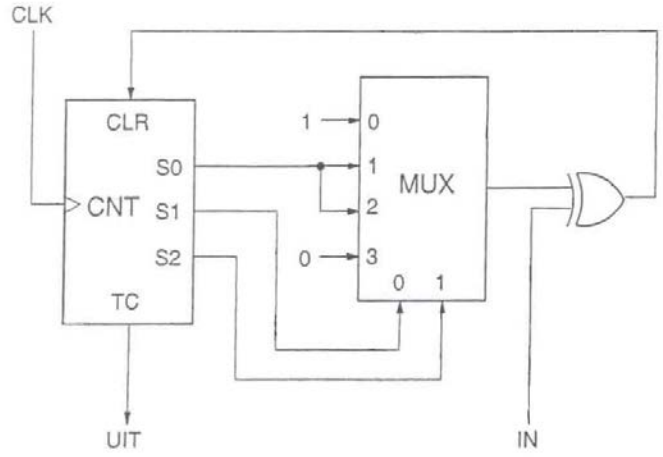


Van een schakeling opgebouwd uit 3 JK FLIP-FLOPS C, B en A en een ingangssignaal S is het gecodeerde toestandsdiagram hiernaast gegeven. Uit de co-deringen CBA is te zien dat C en B direct bestuurd worden door respectivelijk B en A (schuifregistersekties). Bepaal de sturing van de JK FLIP-FLOP A.

	J	K
a.	$S.(C'+ B')$	$S'.C'+ B.C$
b.	$C'+ B'$	$S'.C'+ B.C$
c.	$C'+ B'$	$(S + C).(B'+ C')$
d.	$S.(C'+ B')$	$(S + C).(B'+ C')$

(English: Of a circuit comprising 3 JK flip-flops C, B, and A and an input signal S, the coded state diagram is given above. From the coding of CBA, we can observe that C and B are directly controlled by B and A (shift register sections). Derive the control of JK flip-flop A.)

Opgave 13: (Question 13)



Het gegeven schema bestaat uit een 3-bits binaire teller, een multiplexer met 4 data-ingangen, en een poort. De CLR-ingang van de teller is synchroon, dus het resetten wordt pas geëffectueerd op de klokpuls. Als de teller wordt gestart in de 0 0 0 stand, welke ingangsbitreeks $b_0\ b_1\ b_2$ •••• $b_5\ b_6$ zal een 1 bij de uitgang UIT geven? (S0 is het laagstwaardige bit van de teller)

(English: The given circuit comprises a 3-bit binary counter, a multiplexer with 4 data inputs, and a gate. The CLR input of the counter is synchronous meaning that the reset is only effected on the clock pulse. If the counter is starting in the 0 0 0 state, which input sequence $b_0\ b_1\ b_2$ •••• $b_5\ b_6$ will result in a '1' at the UIT output? (S0 is the least significant bit of the counter)

a. 1 1 0 1 0 1 0
b. 1 1 0 0 0 1 0
c. 1 1 0 0 1 1 0
d. 1 1 0 1 1 1 0

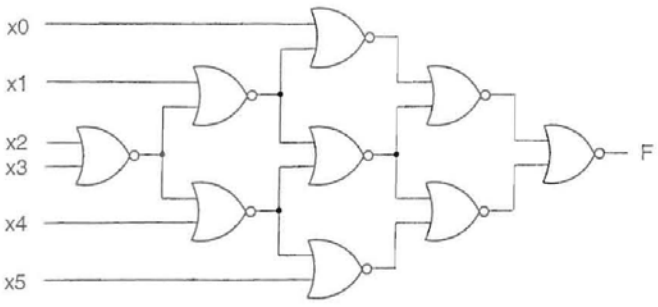
Opgave 14: (Question 14)

Iemand slaat bij het opschrijven van een **hexadecimaal** getal één cijfer over en krijgt daardoor 14080_{10} (decimaal) te weinig. Welk cijfer heeft hij overgeslagen?

(English: Someone erroneously skips a digit when writing down a hexadecimal value and as a consequence receives less of the amount of 14080_{10} (decimal). Which digit did he skip?)

a. 9 b. A c. B d. C

Opgave 15: (Question 15)

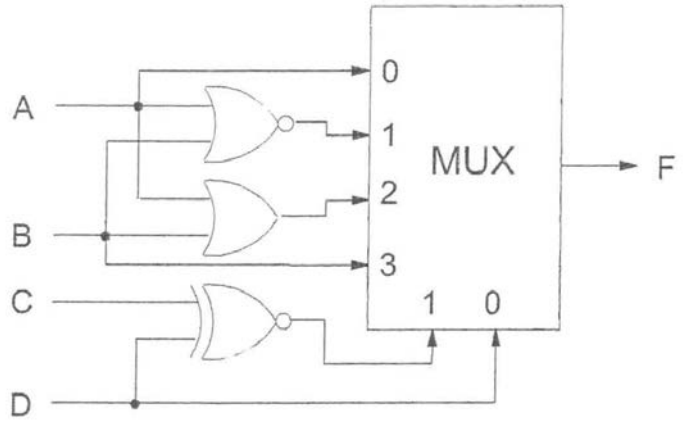


Bepaal de F(x5,x4,x3,x2,xl,x0) van nevenstaand poortnetwerk.

(English: Determine F(x5,x4,x3,x2,xl,x0) of the given gate network.)

a. x0'+ x5'+ xl.x4.(x2'+x3')
b. x0'.x5'+ xl.x4
c. x1 + x4 + x0'.x5'+ x2'.x3'
d. x2'.x3' + x1.x4

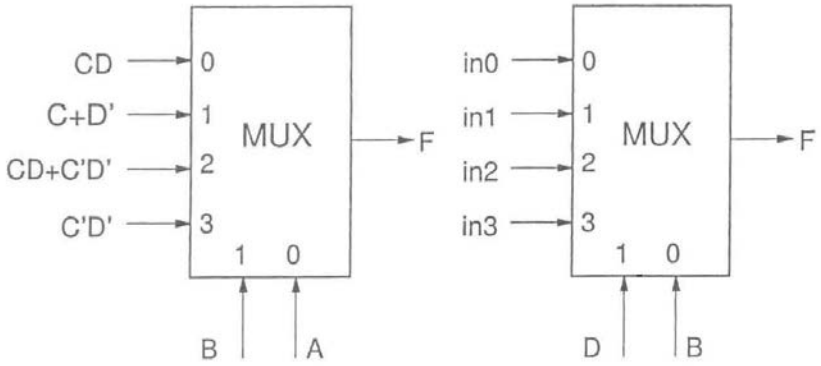
Opgave 16: (Question 16)



Bepaal de mintermvorm van F(D,C,B,A):
(English: Determine F(D,C,B,A) in terms of minterms:)

a. Σ m(1,2,3,5,7,8,14,15)
b. Σ m(1,3,5,6,7,10,11,12)
c. Σ m(1,3,5,6,7,8,14,15)
d. Σ m(1,2,3,5,7,9,11,13,14,15)

Opgave 17: (Question 17)



Met behulp van een multiplexer wordt de functie F(A,B,C,D) gemaakt. Wat moet er als in2 worden aangeboden om voor beide MUX schakelingen identieke uitgangen F(A,B,C,D) te realiseren ?

(English: Using a multiplexer, the function F(A,B,C,D) is realized. What needs to be provided at input in2 to ensure that both MUXes realize the same function F(A,B,C,D)?)

a. C’ b.C c. A’C d. A

Opgave 18: (Question 18)

Wat is de formule van het netwerk wat voor een T-flipflop gezet moet worden om er een JK-flipflop van te maken ?
(English: What is the expression of the network that needs to be placed in front of a T-flipflop in order to simulate a JK-flipflop?)

a. T(t) = j(t).Q'(t) + k'(t).Q(t)
b. T(t) = j(t).Q'(t) + k(t).Q(t)
c. T(t) = k(t).Q'(t) + j'(t).Q(t)
d. T(t) = k(t).Q'(t) + j(t).Q(t)

Opgave 19: (Question 19)

De functie f = (a + b) ⊕ (c + d) is in de mintermvorm te schrijven als:
(English: The function f = (a + b) ⊕ (c + d) can be written in minterm notation as:)

a. f(d,c,b,a) = Σ m(5,6,7,9,10,ll,13,14)
b. f(d,c,b,a) = Σ m(1,2,4,5,6,8,9,10)
c. f(d,c,b,a) = Σ m(5,6,9,10,13,14,15)
d. f(d,c,b,a) = Σ m(1,2,3,4,8,l2)

Opgave 20: (Question 20)

Gegeven zijn de volgende processen:
(English: Given the following processes:)

```
proc1:     process (x,y,z) is  -- Process 1
           variable var_s1 : std_logic;
           begin
                L1: var_s1 := x and y;
                L2: res1 := var_s1 nor z;
           end process;

proc2:     process (x,y,z) is  -- Process 2
           begin
                L3: sig_s1 <= x and y;
                L4: res2 <= sig_s1 nor z;
           end process;
```

De waarden van de signalen voordat de processen starten, zijn als volgt: x = ‘1’, y = ‘1’, z = ‘0’, sig_s1 = ‘0’. Wat is de waarde van ‘res’ na executie van beide processen?
(English: The values of the signal before the processes start are: x = ‘1’, y = ‘1’, z = ‘0’, sig_s1 = ‘0’. What are the values of ‘res1’ and ‘res2’ after the execution of both processes?

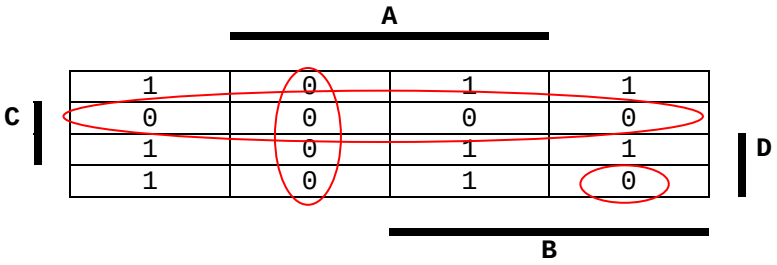
	Process 1	Process 2
a.	0	0
b.	1	0
c.	0	1
d.	1	1

Antwoorden en Uitwerkingen (Answers)

Opgave		Opgave		Opgave		Opgave	
1	A	6	C	11	A	16	A
2	D	7	C	12	B	17	B
3	D	8	C	13	A	18	B
4	B	9	D	14	B	19	D
5	C	10	D	15	D	20	C

Question 1: (a)

The function is already written using maxterms, therefore we can quickly derive the following Karnaugh-map:



By coincidence, the three maxterms happen to be prime implicates and since all of them contain non-covered zeroes, they are also essential.

Question 2: (d)

Question 3: (d)

Answer a is incorrect, because variables are also allowed in processes.
Answer b is incorrect, because variables also occur in processes (therefore, outside of functions and procedures).
Answer c is incorrect, because variables do not have a time component.

Question 4: (b)

tpLH(C→F) = tpLH(OR-2)+tpLH(AND-2)+tpLH(INV)+tpHL(NOR-3)+tpLH(AND-2) =
=(0.12+0.037)+ (0.15+0.037)+(0.02+0.038)+(0.08+0.034)+(0.15+0.037)=
=0.157+0.187+0.058+0.114+0.187=0.703 ns

Question 5: (c)

	A'+B.C	*D*	*Not (C)*	*A xor B*	*A xnor B*
Cycle #	**D**	**C**	**B**	**A**	**Z**
0	0	0	0	1	**0**
1	0	0	1	1	**0**
2	0	0	1	0	**0**
3	1	0	1	1	**0**
4	0	1	1	0	**0**
5	1	0	0	1	**0**
6	0	1	1	1	**0**
7	1	0	0	0	**1**
8	1	1	1	0	**0**
9	1	1	0	1	**0**
10	0	1	0	1	**0**
11	0	0	0	1	**0**

From this table, you can derive that the answer should be 11 cycles.

Question 6: (c)

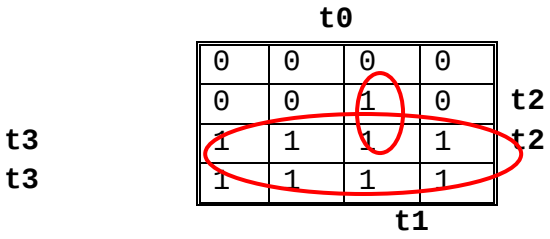
1/(10+4+5=19 ns) = 52 MHz → 50 MHz is de maximum frequency.

Question 7: (c)

We need to build a 16Mx16 memory system. 10 bits of the address lines go to the memory elements themselves and the remainder 4 bits need to be decoded to go to one of the 16 rows of 1M memories → see Figure 9.8 in book.

Question 8: (c)

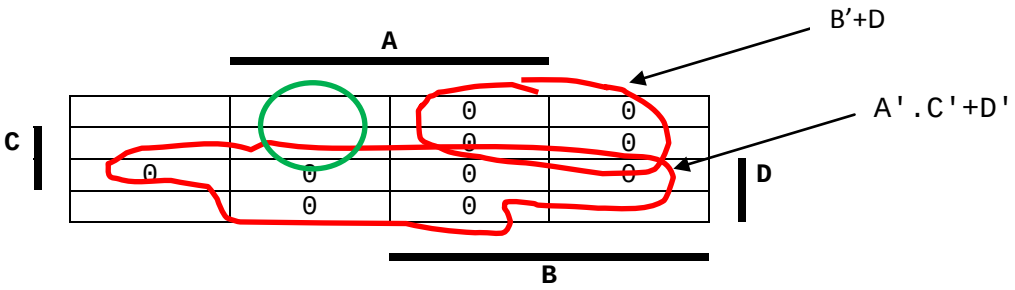
F3 = ((t0 + t3)' + (t3 + t1.t2)')' (de Morgan)
F3 = (t0 + t3).(t3 + t1.t2) (distributivity)
F3 = t0.t3 + t3 + t0.t1.t2 + t1.t2.t3 (absorption : a +ab = a)
F3 = t3 + t0.t1.t2 + t1.t2.t3 (absorption)
F3 = t3 + t0.t1.t2



This is the Karnaugh map of the function m(7,8,9,10,11,12,13,14,15) and corresponds to the control of the Red light of traffic light L0.

Question 9: (d)

Note: the enable input of the tri-state buffers are inverted. Therefore, we need to know when functions F1 and F2 are zero. This results in the following Karnaugh map:



The answers can be read as maxterms (zeroes) and these can be placed inside the drawn Karnaugh map. We can derive now that the answer A'+B+D is the only answer that does not overlap with those of F1 and F2.

Question 10: (d)

J	PS (D C B A)	NS (D C B A)
0	0 0 0 0	-
1	0 0 0 1	1 0 1 **0**
2	0 0 1 0	1 1 0 **0**

3	0 0 1 1	1 1 1 **0**
4	0 1 0 0	**-**
5	0 1 0 1	0 1 1 **1**
6	0 1 1 0	0 0 0 **1**
7	0 1 1 1	0 0 1 **1**
8	1 0 0 0	**-**
9	1 0 0 1	0 0 1 **0**
10	1 0 1 0	0 1 0 **1**
11	1 0 1 1	0 1 1 **0**
12	1 1 0 0	1 1 0 **1**
13	1 1 0 1	1 1 1 **1**
14	1 1 1 0	1 0 0 **1**
15	1 1 1 1	1 0 1 **1**

A

C				**D**
-	0	0	0	
-	1	1	1	
1	1	1	1	
-	0	0	1	

B

We can derive from this that the expression is:
C + A'.D

Question 11: (a)

1-equivalent: (A, B, C, E, F, G, H, I, J) (D)
2-equivalent: (A, C, H, I, J) (B, E, F, G) (D)
3-equivalent: (A, C, I) (H, J) (B, E, F, G) (D)
We can observe that only H and I are 2-equivalent and not 3-equivalent.

Question 12: (b)

	Previous State			Inputs	
J	**C**	**B**	**A**	**S=0 (C B A)**	**S=1 (C B A)**
0, 8	0	0	0	0 0 **1**	0 0 **1**
1, 9	0	0	1	0 1 **0**	0 1 **1**
2, 10	0	1	0	1 0 **1**	1 0 **1**
3, 11	0	1	1	1 1 **0**	1 1 **1**
4, 12	1	0	0	0 0 **1**	0 0 **1**
5, 13	1	0	1	0 1 **1**	0 1 **1**
6, 14	1	1	0	1 0 **0**	1 0 **0**
7, 15	1	1	1	1 1 **0**	1 1 **0**
				Next State	

A_{new}: (met S als hoogstwaardige bit)

A_{oud}

C				**S**
1	0	0	1	
1	1	0	0	
1	1	0	0	
1	1	1	1	

B

$J_{new}(A)$: = C'+B'

C	A_{oud}			S
1	-	-	1	
1	-	-	0	
1	-	-	0	
1	-	-	1	
	B			

$K_{new}(A)$: = C'.S'+C.B

C	A_{oud}			S
-	1	1	-	
-	0	1	-	
-	0	1	-	
-	0	0	-	
	B			

Question 13: (a)

The purpose is to force the counter to reach the 1 1 1 state in order to generate the TC. Consequently, we need to ensure with the input that the CLR signal is not generated.

				0	*S0*	*S0*	*1*	*S2*	*S1*		**IN**
X	**S2**	**S1**	**S0**	**3**	**2**	**1**	**0**	**1**	**0**	**Exor**	**b_x=?**
0	0	0	0	0	0	0	**1**	0	0	1 ⊕	**1**
1	0	0	1	0	1	1	**1**	0	0	1 ⊕	**1**
2	0	1	0	0	0	**0**	1	0	1	0 ⊕	**0**
3	0	1	1	0	1	**1**	1	0	1	1 ⊕	**1**
4	1	0	0	0	**0**	0	1	1	0	0 ⊕	**0**
5	1	0	1	0	**1**	1	1	1	0	1 ⊕	**1**
6	1	1	0	**0**	0	0	1	1	1	0 ⊕	**0**

Question 14: (b)

$(C_{n-1} .. C_{x+1} C_x C_{x-1} .. C_0) - (C_{n-1} .. C_{x+1} C_{x-1} .. C_0) = 14080_{10}$

$((C_{n-1} .. C_{x+1} C_x) - (C_{n-1} .. C_{x+1})) * 16^x = 14080_{10}$ (x=1, not divisable by16^1 of 16^2)

$C_{n-1}*16^{n-1} + (C_{n-2}-C_{n-1})*16^{n-2} +..+ (C_3 - C_4)*16^3 + (C_2 - C_3)*16^2 + (C_1 - C_2)*16 = 14080_{10}$

$C_{n-1}*16^{n-2} + (C_{n-2}-C_{n-1})*16^{n-3} +..+ (C_3 - C_4)*16^2 + (C_2 - C_3)*16^1 + (C_1 - C_2) = 880_{10}$

$(C_{n-1}-C_{n-1})*(16^{n-2}-16^{n-3}) +..+ C_{x+2}*(16^2-16^1) + C_{x+1}*(16^1-1) + C_x = 880_{10}$

$(C_{n-1}-C_{n-1})*(16^1-1)*16^{n-3} +..+ C_{x+3}*(16^1-1)*16^2 + C_{x+2}*(16^1-1)*16 + C_{x+1}*(16^1-1) + C_x = 880_{10}$

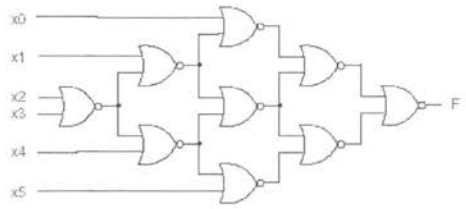
$(C_{n-1} .. C_{x+3} C_{x+2} C_{x+1})(16-1) + C_x = 880_{10}$

➔ $(C_{n-1} .. C_{x+3} C_{x+2} C_{x+1})$ is another number in hexadecimal representation. We now have to subtract a value * 15(=16-1) from 880 → Modulo operation

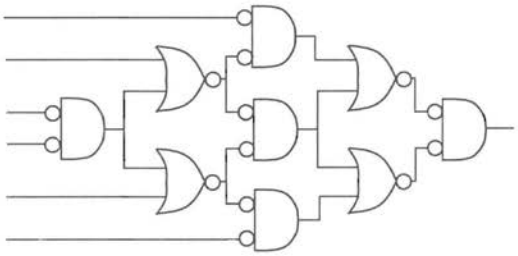
$C_x = 880_{10}$ (mod 15) = 10_{10} = A

Question 15: (d)

The original circuit can be transformed to the following circuit by applying the DeMorgan's law several times:

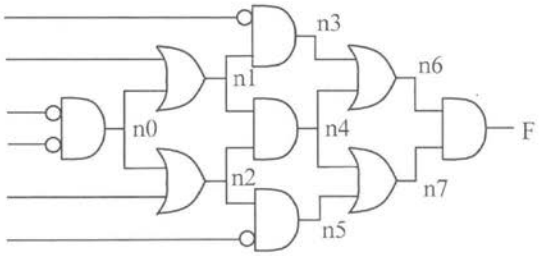


$F = n6.n7 = (n3 + n4).(n4 + n5)$
$F = n3.(n4 + n5) + \mathbf{n4}.(\mathbf{n4} + n5)$
$F = n3.(n4 + n5) + n4$
$F = n3.n5 + n3.\mathbf{n4} + \mathbf{n4}$
$F = n3.n5 + n4$



$n4 = n1.n2$
$n3 = x0'.n1$
$n5 = x5'.n2$

$F = (x0'.n1).(x5'.n2) + n1.n2$
$F = x0'.x5'.n1.n2 + n1.n2$
$F = n1.n2$



$F = (x1 + x2'.x3').(x4 + x2'.x3')$
$F = x1.(x4 + x2'.x3') + x2'.x3'.(x4 + x2'.x3')$
$F = x1.(x4 + x2'.x3') + x2'.x3'$
$F = x1.x4 + x1.x2'.x3' + x2'.x3'$
$F = x1.x4 + x2'.x3'$

$\Rightarrow$ **d.**

Question 16: (a)

					Selectors		Mux Inputs				
					C xnor D	*D*	*A*	*A nor B*	*A or B*	*B*	
J	**D**	**C**	**B**	**A**	**1**	**0**	**0**	**1**	**2**	**3**	**F**
0	0	0	0	0	1	0			0		0
1	0	0	0	1	1	0			1		1
2	0	0	1	0	1	0			1		1
3	0	0	1	1	1	0			1		1
4	0	1	0	0	0	0	0				0
5	0	1	0	1	0	0	1				1
6	0	1	1	0	0	0	0				0
7	0	1	1	1	0	0	1				1
8	1	0	0	0	0	1		1			1
9	1	0	0	1	0	1		0			0
10	1	0	1	0	0	1		0			0
11	1	0	1	1	0	1		0			0
12	1	1	0	0	1	1				0	0
13	1	1	0	1	1	1				0	0
14	1	1	1	0	1	1				1	1
15	1	1	1	1	1	1				1	1

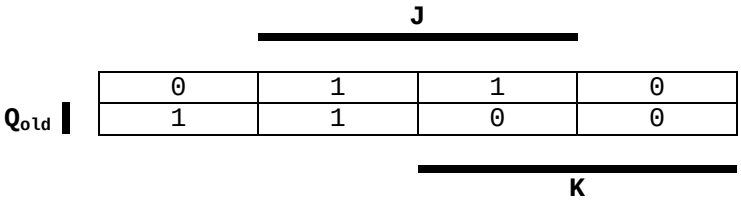
Concluding: Σ m(1,2,3,5,7,8,14,15)

Question 17: (b)

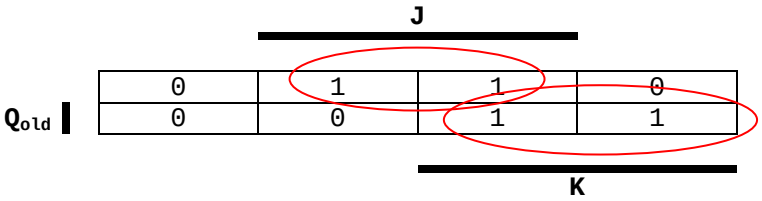
A'.B'.C.D + A.B'.(C+D') + A'.B.(C.D+C'D') + A.B.C'.D' from the left MUX.
For in2, we need to fill in: D=1 en B=0 → A'C + A.C = (A'+A).C = C

Question 18: (b)

Q_{new}: (using JK)



Qnew: (rewritten to a T-flipflop)



We obtain: j(t).Q'(t)+k(t).Q(t)

Question 19: (d)

J	d c b a	(a + b)	(c + d)	(a + b) ⊕ (c + d)
0	0 0 0 0	0	0	0
1	0 0 0 1	1	0	1
2	0 0 1 0	1	0	1
3	0 0 1 1	1	0	1
4	0 1 0 0	0	1	1
5	0 1 0 1	1	1	0
6	0 1 1 0	1	1	0
7	0 1 1 1	1	1	0
8	1 0 0 0	0	1	1
9	1 0 0 1	1	1	0
10	1 0 1 0	1	1	0
11	1 0 1 1	1	1	0
12	1 1 0 0	0	1	1
13	1 1 0 1	1	1	0
14	1 1 1 0	1	1	0
15	1 1 1 1	1	1	0

Dus: f(d,c,b,a) = Σ m(1,2,3,4,8,l2)

Question 20: (c)

var_s1 := '1' and '1' := '1' → res1 := '1' nor '0' := '0'
res2 <= '0' nor '0' (= '1')