ET8 019 – Computer Arithmetic

Exam 18.04.2012 9:00-12:00

- The exam is **open book** thus you can use the *course book*, the *slides*, and any other book on computer arithmetic and logic design.
- *Laptops*, *smartphones*, etc., with or without wireless connection, and all kind of personal notes including example *exams/problems with solutions* **cannot** be utilized during the exam.
- The exam consists of 11 questions, the points per question are given between parentheses, and the total amount of points one may get is 100.
- Do not forget to write your name and study number on the answers and to fill in the evaluation form (when available).

Good luck!

1. (10p) Consider a number system with r = 6 and the digit set [-3, 5]. Find the relevant parameters for a carry-free addition in this system. For such a system, assuming that the digits in position i are x_i and y_i, the position sum is $p_i = x_i + y_i$, and the interim sum $w_i = p_i - 6t_{i+1}$. Deduce the logic equations for the circuit that produces the transfer digit t_{i+1}.

2. (5p) Consider the Residue Number System RNS(16|15|10), which is the equivalent of a k-bit unsigned number system.

   a. Which is the actual value of k?
   b. Represent the numbers x = 50 and y = - 25 in this system.
   c. Compute x + y. Comment on the obtained result.

3. (17p) Assume that Boolean gates, full adders, 2:1 multiplexers, and 4-bit look-ahead carry circuits are available. Make you own (plausible) assumptions about the cost and area of each such building block. Draw the organization and compare the following adders, to be utilized as significant adder in an IEEE single precision floating point unit, in terms of cost and delay:

   a. Carry look-ahead adder.
   b. Single-level carry select adder.
   c. Two-level carry select adder.
   d. Optimal variable-block carry-skip adder.

4. (8p) Draw the prefix graph for a 28-bit hybrid carry network built with two levels of the Brent-Kung scheme at each end and the rest with Kogge-Stone.

5. (15p) Design a Mod-9 adder and a Mod-9 multiplier required for the implementation of an RNS system with a Mod-9 channel. You may make use of full/half adders and NAND gates (no other components are allowed).

6. (10p) Design a (3, 3, 3; 5)-counter using full adders and half adders as building blocks with the least possible delay. Use such counters to reduce four 9-bit numbers to two rows while minimizing the cost and delay.

7. (10p) A 6 x 2 AMM computes an 8-bit value $p = a \cdot x + b + y$, where a and b (x and y) are 6-bit (2-bit) unsigned numbers.

    a. Implement the 6x2 AMM with full adders and half adders while optimizing the delay.
    b. Using the dot notation show how such AMMs can be used to build 6 x 6 AMM having two 6-bit multiplicative and two 6-bit additive inputs and producing a 12-bit result. Minimize the number of used 6 x 2 AMMs.

8. (10p) Given the dividend z =+.1010 and the divisor d = -.1101 in sign-magnitude representation. Represent them in 5-bit 2's complement format and then perform the division using the non-restoring algorithm. Convert the quotient into 2's complement format.

9. (5p) Compare a radix-4 SRT division with quotient digit set [-3,3] with the one with quotient digit set [-2,2]. Briefly highlight the advantages and disadvantages of each scheme.

10. (5p) What is the decimal value of the following single precision (IEEE standard compliant) floating point number X = (1100 0101 1101 0000 0000 0000 0000 0000)? Detail the way you obtained the decimal value of X.

11. (5p) Compare floating-point number systems with fixed/floating-slash number systems. Briefly highlight the advantages and disadvantages of each scheme.