Embedded	Computer	Architectures	II	(192130250)	)

Wednesday 30 January 2013 15 pages with 6 problems

## Guidelines for the exam:

- 1. Answers have to be written down at the appropriate places in this questionnaire.
- 2. Fill in your name, studentnumber and study-programme.
- 3. Hand in all pages.
- During the exam, the use of books and electronic equipment (laptop, organizers, mobile phones) is prohibited

Name:	
Studentnumber:	 Study-programme:

QUESTION 1

(8+2+7+10+3=30 POINTS)

A palindrome is a word that is equal when read from left to right and from right to left. An example is the word 'redivider'.

We want to design a fast circuit that recognizes palindromes of length 2L+1 (hence, of odd length where L is given) in an arbitrary stream of data, for example for recognizing 'redivider' in the sentence ".... the government as a redivider of money ....".

The input datastream consists of data-elements  $x_i$ , where  $-\infty < i < \infty$ .

The output is a stream of Boolean values  $c_i$ , where  $-\infty < i < \infty$ .

An output value  $c_i$  is true if and only if the datastream contains a palindrome of length 2L+1 'around  $x_i$ ', e.g.,  $x_{i-1}=x_{i+1}$ ,  $x_{i-2}=x_{i+2}$ ,  $x_{i-3}=x_{i+3}$ , and so on. So, the algorithm is described by

$$c_i = \bigwedge_{k=1}^{L} (x_{i-k} = x_{i+k})$$

Hint: The operator  $\wedge_{k=1}^{L}$  has the same meaning w.r.t. *logical and* ( $\wedge$ ) as the well known operator  $\sum_{k=1}^{L}$  w.r.t. *addition* (+). We remark that both " $\wedge$ " and "+" are associative and commutative, thus both have the same level of freedom in the design.

	the horizontal direc	

Below a possible architecture to recognize palindromes (for the case L=3) is described by means of a functional program pal (short for "palindrome"):

In this definition the *state* consists of two lists (us, ts) of registers, and x is the next input value. The value last ts' is the next output of the architecture, and (x+>>us, True+>>ts') is the next state. Remember that last returns the last element of a list, and +>> adds an element x to the beginning of a list, throwing away the last element.

The function **zipWith** combines two lists elementwise, by means of a given operator (in this case the boolean functions for equality and for logical and), and the operation !!! returns the list of elements 1, 3, 5 from the list us (remember that the first element of a list is number zero). Finally, the function **replicate** repeats a value (here x) a given number of times (here 3).

e)	Indicate the projection- and scheduling vector that should be used on your dependency graph to							
	obtain the architecture of question 1d. Write down the vect	ors as follows: $\binom{i}{k}$	where 'i' indicates					
	the vertical dimension and 'k' the horizontal dimension.							
	Projection vector							
	Scheduling vector							

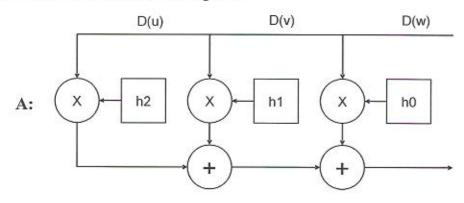
QUESTION 2	(8+5+5+7=25  POINTS)
infinite stream of values indicated by $x$ and $h$	th two inputs and one output. The two inputs receive an respectively. The output delivers a stream of values and output is given by the following expression
$y_z = \sum_{i=0}^{N-1} x_z . h_{z+i}$	
We assume that $z$ indicates discrete time, so $y$	$y_z$ comes after $y_{z-l}$ . Similar reasoning is valid for $x$ en $h$ .
<ul> <li>a) Give the set of recurrent relations the dependencies.</li> </ul>	nat describes the algorithm completely. Use global

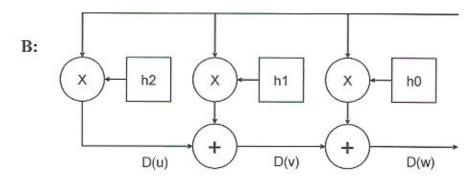
Draw the depend	ency graaf with glob	oal dependencies.	Indicate the varia	bles in the graph.	

Give the set dependencies				9	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	 	

QUESTION 3 (5 POINTS)

Below, the filter circuits A and B are given:.





Both circuits have the same behavior. The following function definitions are given:

f1 (State 
$$[u, v, w]$$
) x = (State  $[u*h2, v*h1, w*h0]$  ,  $u*x+v*x+w*x$ )

f2 (State 
$$[u, v, w]$$
)  $x = (State [x*h2, u+x*h1, v+x*h0], w)$ 

f3 (State 
$$[u, v, w]$$
) x = (State  $[x*h2, x*h1, x*h0]$  ,  $u+v+w$ )

f4 (State 
$$[u,v,w]$$
)  $x = (State [v,w,x]$  ,  $u*h2+v*h1+w*h0$ )

The circuits A and B are described by one of the pairs of functions below (the first function describes A, the second describes B).

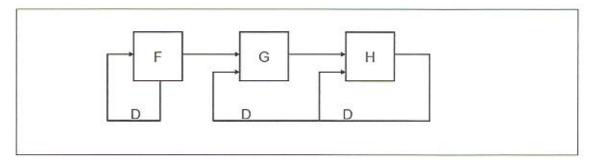
Which of the pairs below is correct?

- (1) f2, f1
- (2) f4, f2
- (3) f1, f3
- (4) f3, f4

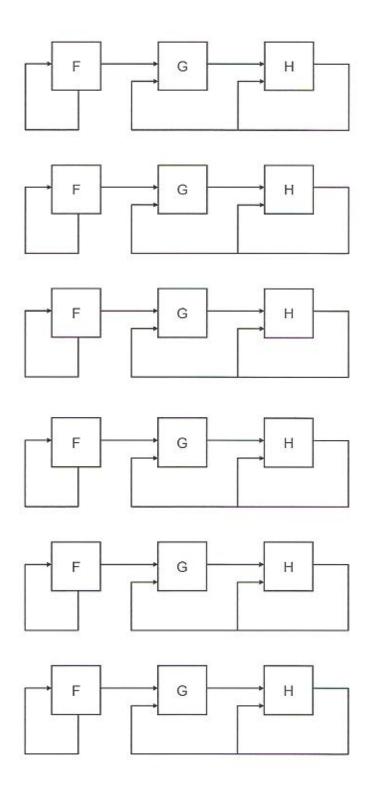
QUESTION 4

(8 PUNTEN)

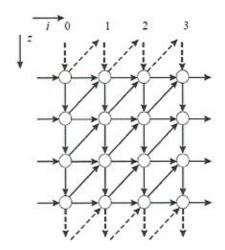
Below, the following signal flow graph is given:



Deduct by means of retiming from this signal flow graph a systolic signal flow graph which means that each output should be accompanied by a delay element. Use the template below and show all intermediate steps.



Given is the dependency graph below, where  $(-\infty < z < \infty \quad and \quad 0 \le i \le 3)$ 



a) What (are) is the possible direction(s) of the projection vector(s)?

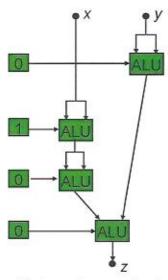
b) What (are) is the possible direction(s) of the scheduling vector(s)? Present this in the following format example:  $\binom{i}{i} = \binom{-3}{-1}$  to  $\binom{2}{-1}$  clockwise

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c) Make a drawing of the signal flow graph in case the projection vector equals  $\binom{i}{j} = \binom{1}{0}$  and the scheduling vector equals  $\binom{i}{j} = \binom{1}{2}$ . Annotate the signal flow graph with the indices of the nodes and the delay operators D.

QUESTION 6 (12 PUNTEN)

Below, a dependency graph is given:



To map this dependency graph onto a processor-like architecture, the graph must be made time shift invariant.

Using the dependency graph above, determine the time shift invariant dependency graph. Indicate clearly the time zones that are introduced and the decoders and multiplexers to be used. Also indicate the control of the decoders and multiplexers. Use the templates below (multiple templates are given to illustrate the intermediate steps).







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