

# Midterm Computer Organisation TI1406

**Please read the following information carefully!**

- This exam consists of 10 multiple-choice questions. Each question is worth 300 points.
- You have 60 minutes to complete this exam.
- Before you hand in your answers, check that your multiple-choice form contains your name and student number, also filled in using the boxes.
- Opening this exam before you are instructed to start is **strictly prohibited**.
- The use of the book, notes, calculators, smartwatches and other aids is **strictly prohibited**.
- Note that the order of the letters next to the boxes on your multiple-choice sheet may **not always be A-B-C-D!**
- Tip: mark your answers on this exam **first**, and only after you are certain of your answers, copy them to the multiple-choice answer form.

1. You decide to have lunch from “Broodje Leo” with your mentor group and even bring one for your teacher. Your order is shown in the table below. How much is the order total in two's complement?

| Amount | Type                             | Cost (€)               | Number system |
|--------|----------------------------------|------------------------|---------------|
| 4      | “Kwalileo” Ciabatta              | 0 10000000 10100 ... 0 | IEEE-754      |
| 8      | Pistolet ham & cheese            | 0000 0011              | S&M           |
| 1      | Ciabatta with “Kip Kerrie” salad | 0000 0100              | 1C            |
| 1      | Group discount                   | 0010 0010              | excess-42     |

Table 1: Your order

- A. 0001 0001  
 B. 0010 0001  
 C. 0010 1001  
 D. 0010 1010
2. Assume a 64 bit processor with 42 registers and 3 addressing modes (immediate, direct and register). For simplicity all instructions are 128 bits long. This processor supports 142 instructions and a byte addressable memory up to 4 TB.  
 How many bits can your immediate values be for instructions with 2 registers, one immediate and one direct operand?
- A. 44 bits  
 B. 66 bits  
 C. 69 bits  
 D. 76 bits
3. See Figure 1. Which of the following functions describes this circuit?

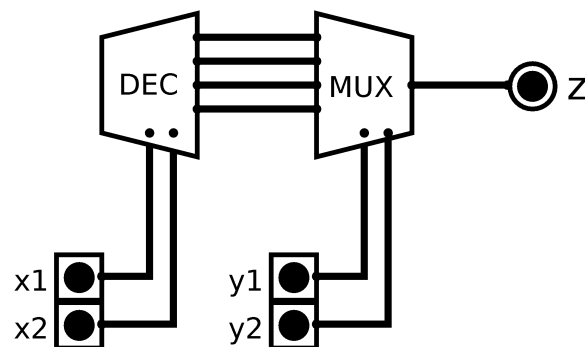


Figure 1

- A.  $z = \overline{x_1} \cdot \overline{x_2} \cdot \overline{y_1} \cdot \overline{y_2}$   
 B.  $z = (\overline{x_1} \cdot y_1 + x_1 \cdot \overline{y_1}) \cdot (x_2 \cdot \overline{y_2} + \overline{x_2} \cdot y_2)$   
 C.  $z = x_1 \cdot x_2 \cdot y_1 \cdot y_2$   
 D.  $z = (\overline{x_1} \cdot \overline{y_1} + x_1 \cdot y_1) \cdot (\overline{x_2} \cdot \overline{y_2} + x_2 \cdot y_2)$

4. Maya has decided to get herself a burger, but unfortunately there is an issue with the cash register of the local burger joint. Due to a hardware bug, floating point numbers are incorrectly converted to decimal numbers. After consulting with the tech-savvy Lisa Basil, they conclude that the cash register has several faults that cause several of the bits in the floating point registers to always be 1.

Maya's regular burger order would normally cost \$5.75, but due to these hardware errors the order costs \$93.50. Which bits in the floating point register are definitely broken, if we count from left to right with  $b_0$  being the sign bit,  $b_1$  the first exponent bit, and  $b_9$  the first mantissa bit.

- A.  $b_6, b_9, b_{10}, b_{13}, b_{15}, b_{16}$
  - B.  $b_6, b_{14}, b_{15}$
  - C.  $b_7, b_9, b_{10}$
  - D.  $b_7, b_{13}, b_{14}$
5. Consider the following logical expression  $S = (a + b) \cdot (b + c) \cdot (\overline{d + a})$ . Which of the variables does not affect the outcome of the expression?
- A. a
  - B. b
  - C. c
  - D. d
6. Let us assume that there are  $1000_8$  students enrolled in a bachelor on a hypothetical university in Unicorn City. We estimate that **half of them** have obtained a bonus 132 (excess-128) times, for  $2C_{16}$  points each time. Given that every 0110 0010 0101 0000 (BCD) points Koen takes a painkiller. How many painkillers has Koen taken?
- A. 6
  - B. 7
  - C. 14
  - D. 15
7. You are asked to design a digital circuit that adds three input bits  $x$ ,  $y$  and  $z$  together. The output of your circuit is a sum bit  $s$  and a carry bit  $c$ . Which of the following formulas can be used to design this circuit?

$$f_1 = \overline{xy}z + \overline{xy}z + \overline{xy}z + \overline{xy}z$$

$$f_2 = xyz + \overline{xy}z + \overline{xy}z + \overline{xy}z$$

$$f_3 = \overline{xy}z + xy\overline{z} + x\overline{y}z + \overline{x}yz$$

$$f_4 = xyz + xy\overline{z} + x\overline{y}z + \overline{x}yz$$

- A.  $s = f_1, c = f_3$
- B.  $s = f_2, c = f_4$
- C.  $s = f_3, c = f_1$
- D.  $s = f_4, c = f_2$

8. The world-famous archaeologist and puzzle solver Professor Layton is out on one of his many adventures when he finds himself confronted with an army of angry robots. Before he escapes this situation in a truly fantastical manner, he has just enough time to remark that this reminds him of the following puzzle.

Long ago there was a robot with a very peculiar chip that allowed the robot to feel emotions. Unfortunately due to a small issue in the design of this chip, every NOR gate in the design causes the robot to feel bad. Consider the logic circuit that is currently implemented using 3 NOR-gates in Figure 2.

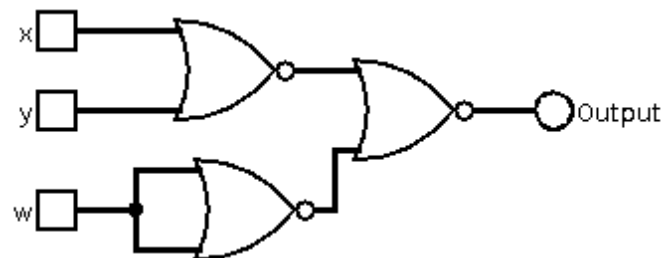


Figure 2

See Figures 3a, 3b, 3c, 3d. Which of these is an equivalent expression implemented using only NAND-gates?

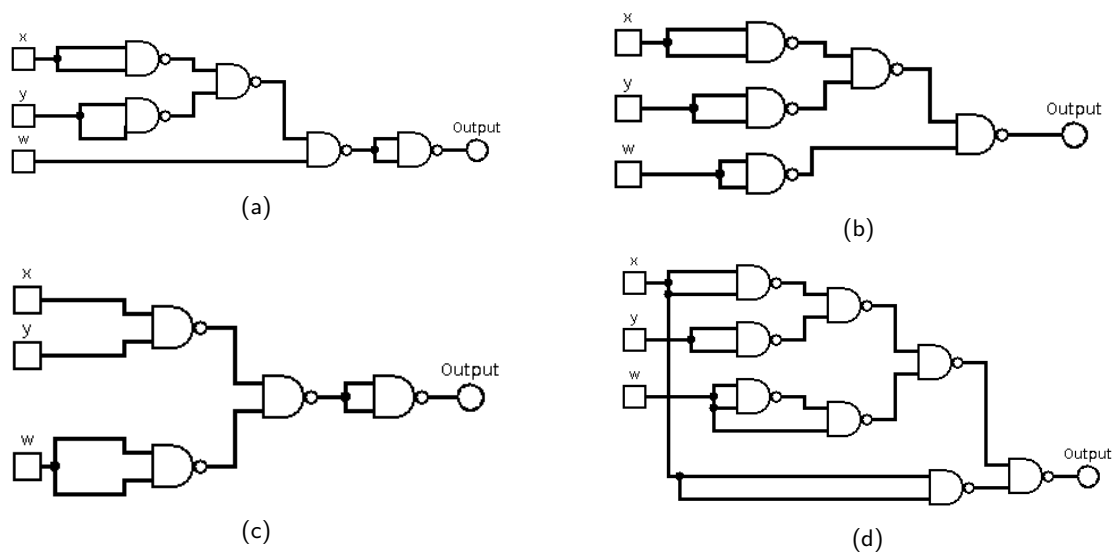


Figure 3

- A. Figure 3a
- B. Figure 3b
- C. Figure 3c
- D. Figure 3d

9. See Figure 4. Otto drew two Karnaugh Maps, but spilled some kerrie on them. The values marked by  $Z$  are no longer readable, but you know that the *minimal sum-of-products* for the maps: (I)  $T=4$ ,  $V=12$  (II)  $T=3$ ,  $V=7$ . For each Karnaugh Map, did  $Z$  contain a 0 or 1?

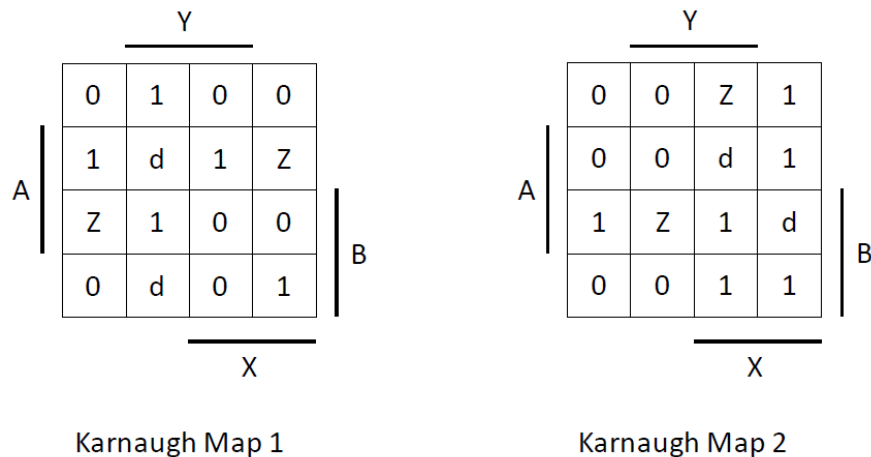


Figure 4

- A. (I)  $Z=0$  (II)  $Z=0$   
 B. (I)  $Z=0$  (II)  $Z=1$   
 C. (I)  $Z=1$  (II)  $Z=0$   
 D. (I)  $Z=1$  (II)  $Z=1$
10. Couple the law with its core element:
- |  |  |
|--|--|
| (A) Moore's Law<br>(B) Rock's Law<br>(C) Law of conservation of misery<br>(D) DeMorgan's Law | (1) Costs<br>(2) Design trade-offs<br>(3) Boolean Algebra<br>(4) Transistors |
|--|--|
- A. (A) - (4); (B) - (2); (C)-(3); (D)-(1);  
 B. (A) - (4); (B) - (2); (C)-(1); (D)-(3);  
 C. (A) - (1); (B) - (4); (C)-(2); (D)-(3);  
 D. (A) - (4); (B) - (1); (C)-(2); (D)-(3);