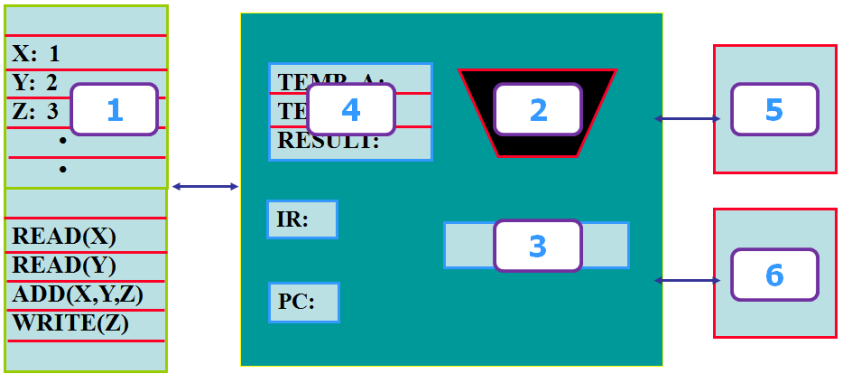
**Exercise 11 (gift)**




This diagram depicts the basic functional units of a computer. What can units 1, 2, 4, and 6 be?

a. 1. Main memory; 2. Registers; 4. ALU; 6. Extended memory.
b. 1. Interconnection network; 2. ALU; 4. Control; 6. Registers.
c. 1. Central Processing Unit; 2. Interconnection network; 4. Timing signals; 6. Main memory.
d. 1. Main memory; 2. ALU; 4. Registers; 6. Interconnection network.

**Exercise 12**

Which of the following statements are correct?

I. Processors with hardwired control are easier to extend with complex instructions than processors with micro-programmed control.

II. Micro-programmed control mechanisms are often implemented using a Programmable Logic Array (PLA).

| | I | II |
|---|---|---|
| a. | correct | correct |
| b. | correct | incorrect |
| c. | incorrect | correct |
| d. | incorrect | incorrect |

**Exercise 13**

Assume the following stack of 64 bit entries:

| address | content |
|---|---|
| x+16 | 3 |
| x+8 | 4567 |
| x | 122 |

and assume the base pointer is at the stack pointer. The assembly program below has issued the instruction "call keyboard_interrupt_top_half". After executing all the instructions until the "ps2" label, what is the content of RAX?

```
main:
      ...
      call  keyboard_interrupt_top_half
      ...

keyboard_interrupt_top_half:
      push  %rbp
      movq  %rsp, %rbp

      sub   8, %rsp
      push  %rdi
      movq  -24(%rbp), %rax
ps2:
      ...
```

a. 3
b. 4567
c. 122
d. Unknown.

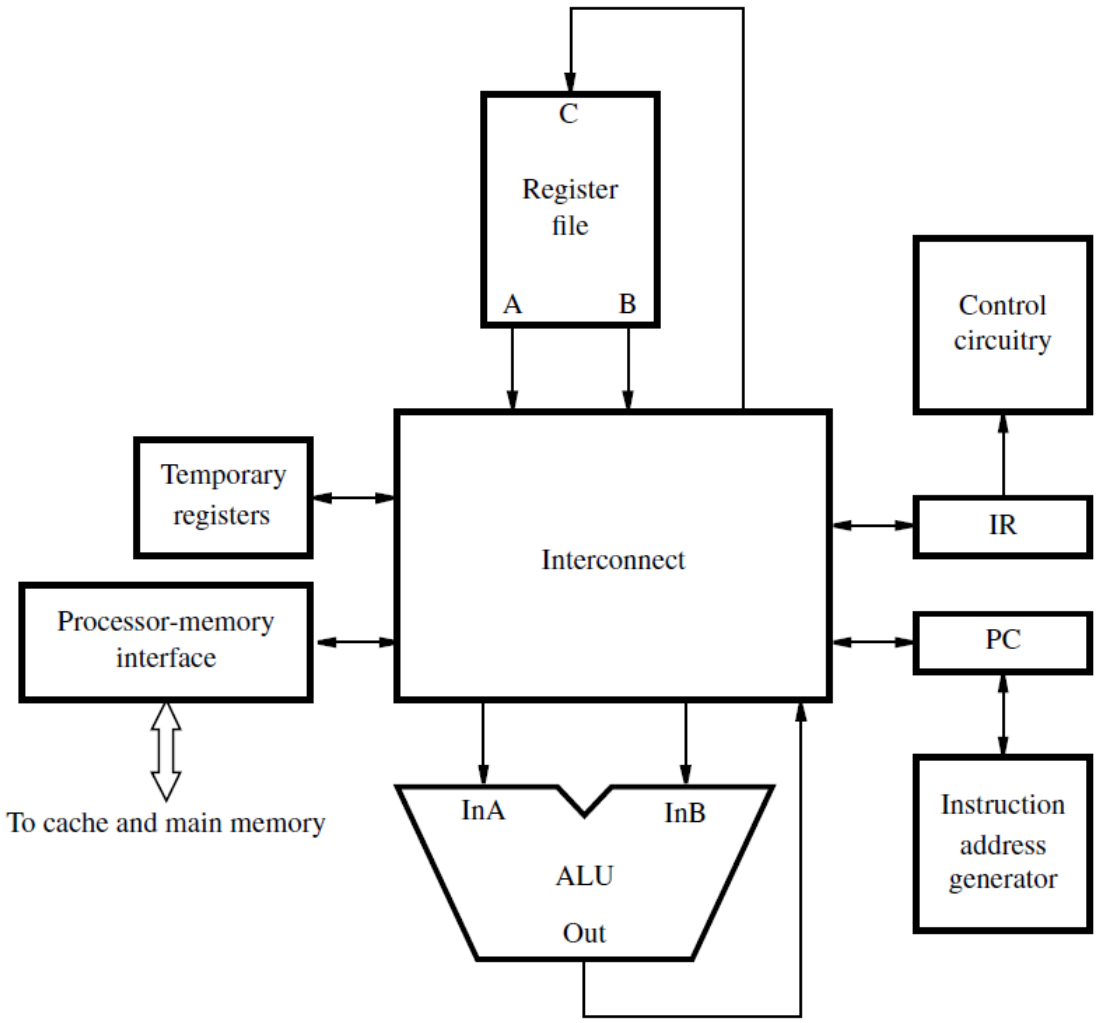
**Exercise 14**

A sound card is connected to the CPU with a bus. The addresses on the bus are 32 bit and the address of the sound card is 0xBEEBBEEB. The sound card ignores address lines 18, 9 and 3. Which of the following does not address the sound card?

a. `0xBEEBBCEB`
b. `0xBEEFBCEB`
c. `0xBEEBBEE3`
d. `0xBEEFBEEF`

**Exercise 15**

Consider the following organization of a CISC processor:




Which of the following statements are true?

I. During program execution, the contents of the PC are regularly moved into the Processor-memory interface.
II. The Control circuitry controls what operation is performed by the ALU.

| | I | II |
|---|---|---|
| a. | correct | correct |
| b. | correct | incorrect |
| c. | incorrect | correct |
| d. | incorrect | incorrect |

**Exercise 16**

Which of the following statements are correct?

I. Cache memories make predicting the execution speed of programs easier.

II. Associative mapping is more flexible than set-associative mapping.

| | I | II |
|---|---|---|
| a. | correct | correct |
| b. | correct | incorrect |
| c. | incorrect | correct |
| d. | incorrect | incorrect |

**Exercise 17**

You have 4 KBytes of byte addressable memory. For this memory, you consider the following organizations:

1. 64-bit words, with a 9-bit address line.
2. 32-bit words, with an 11-bit address line.
3. 16-bit words, with a 10-bit address line.

In which organization(s) is it the case that **not all** words in the memory can be addressed?

a. 1
b. 2
c. 3
d. 2 & 3

**Exercise 18**

A computer with 64 GBytes of main memory, extensible up to 128 GBytes, uses a K-way set-associative cache with 16 MBytes, split into 4096 sets with blocks of 128 Bytes. All memories are word-addressable and have a word length of 32 bits. What are, respectively, the value of K, and the number of bits for the tag (T) and word (W) fields of the memory address?

| | K | T | W |
|---|---|---|---|
| a. | 16 | 19 bits | 6 bits |
| b. | 16 | 18 bits | 6 bits |
| c. | 32 | 18 bits | 5 bits |
| d. | 64 | 17 bits | 5 bits |

**Exercise 19**

Consider the following statements on I/O:

I. Memory mapped I/O consumes roughly 10% of your installed RAM.
II. Port mapped I/O is faster because it uses dedicated ports.

| | I | II |
|---|---|---|
| a. | correct | correct |
| b. | correct | incorrect |
| c. | incorrect | correct |
| d. | incorrect | incorrect |

**Exercise 20**

A team of three anonymous students built a malicious I/O device. They claim that the device and its driver can only access the memory on the device, however in reality the device tries to secretly read passwords from the main memory and pass these on to an external party.

Which of the following statements are correct?

I. Using port mapped memory makes this malicious behaviour more difficult.
II. Reading large amounts of memory to search for passwords can be sped up using DMA.

| | I | II |
|---|---|---|
| a. | correct | correct |
| b. | correct | incorrect |
| c. | incorrect | correct |
| d. | incorrect | incorrect |

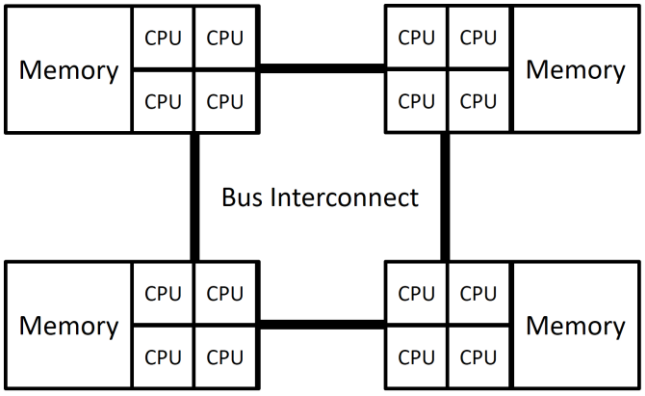
**Exercise 21**

Which of the following performance issues is addressed by introducing **pipelining** in a CPU?

a. Instruction latency.
b. Expensive instructions keep the ALU occupied for multiple cycles.
c. Different functional units inside the CPU are idle during different phases of instruction execution.
d. Branch mispredictions.

**Exercise 22**

Student Thurman buys a new system for rendering her new movie: COMA. It looks like this:

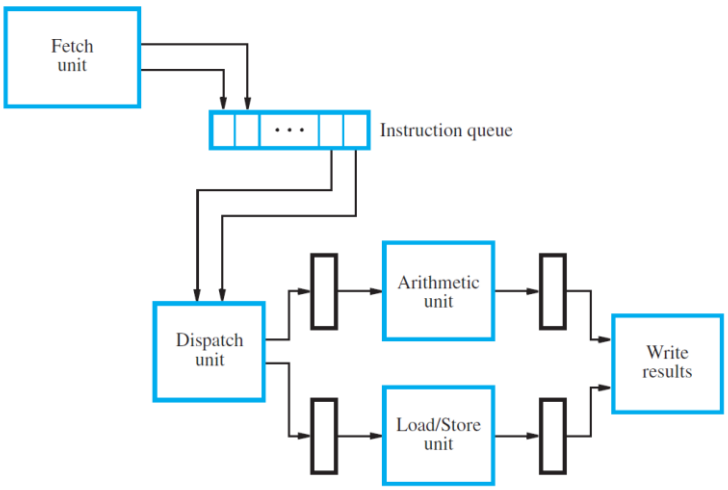



What is the memory architecture used in her system?

a. Message passing
b. UMA
c. NUMA
d. DMA

**Exercise 23**

What can you say with certainty about the CPU shown in the image below?




a. This CPU supports vector instructions.
b. This is a superscalar CPU.
c. This is a dual-core CPU.
d. This CPU supports CISC instructions.

**Exercise 24**

```
for (i = 0; i < N; i++)
    A[i] = B[i] + C[i];
```

(a) A C-language loop to add vector elements

```
        Move            R5, #N          R5 is the loop counter.
LOOP:   Load            R6, (R3)        R3 points to an element in array B.
        Load            R7, (R4)        R4 points to an element in array C.
        Add             R6, R6, R7      Add a pair of elements from the arrays.
        Store           R6, (R2)        R2 points to an element in array A.
        Add             R2, R2, #4      Increment the three array pointers.
        Add             R3, R3, #4
        Add             R4, R4, #4
        Subtract        R5, R5, #1      Decrement the loop counter.
        Branch_if_[R5]> 0 LOOP          Repeat the loop if not finished.
```

(b) Assembly-language instructions for the loop

```
        Move            R5, #N          R5 counts the number of elements to process.
LOOP:   VectorLoad.S    V0, (R3)        Load L elements from array B.
        VectorLoad.S    V1, (R4)        Load L elements from array C.
        VectorAdd.S     V0, V0, V1      Add L pairs of elements from the arrays.
        VectorStore.S   V0, (R2)        Store L elements to array A.
        Add             R2, R2, #4*L    Increment the array pointers by L words.
        Add             R3, R3, #4*L
        Add             R4, R4, #4*L
        Subtract        R5, R5, #L      Decrement the loop counter by L.
        Branch_if_[R5]> 0 LOOP          Repeat the loop if not finished.
```

(c) Vectorized form of the loop

For the sequential and vectorized (parallelized) assembly codes in the figure, assume each instruction takes 1 cycle to execute and N=1,000,000,000 (1 billion).
What is the speedup of vectorization for vector lengths L=2 and L=16?

a. ~1 & ~32
b. ~2 & ~16
c. ~4 & ~8
d. None of the above.

**Exercise 25**

The Aperture Science Company is using a computer program consisting of a sequential and a parallel segment. The program originally took 8 minutes to execute using 1 processor, but Aperture Science has managed to reduce the execution time to 2 minutes by running the same program using 16 processors. How many processors are needed to further reduce the execution time to 1 minute? You may assume that the speedup achieved by this program in practice is equal to the maximum speedup given by Amdahl's Law.

a. Between 17 and 32 processors (inclusive).
b. Between 33 and 64 processors (inclusive).
c. More than 64 processors.
d. The execution time of this program cannot be reduced to 1 minute using any number of processors.

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**End of exam**